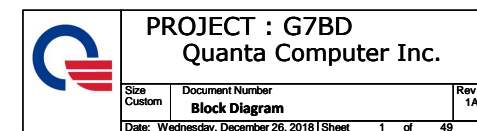


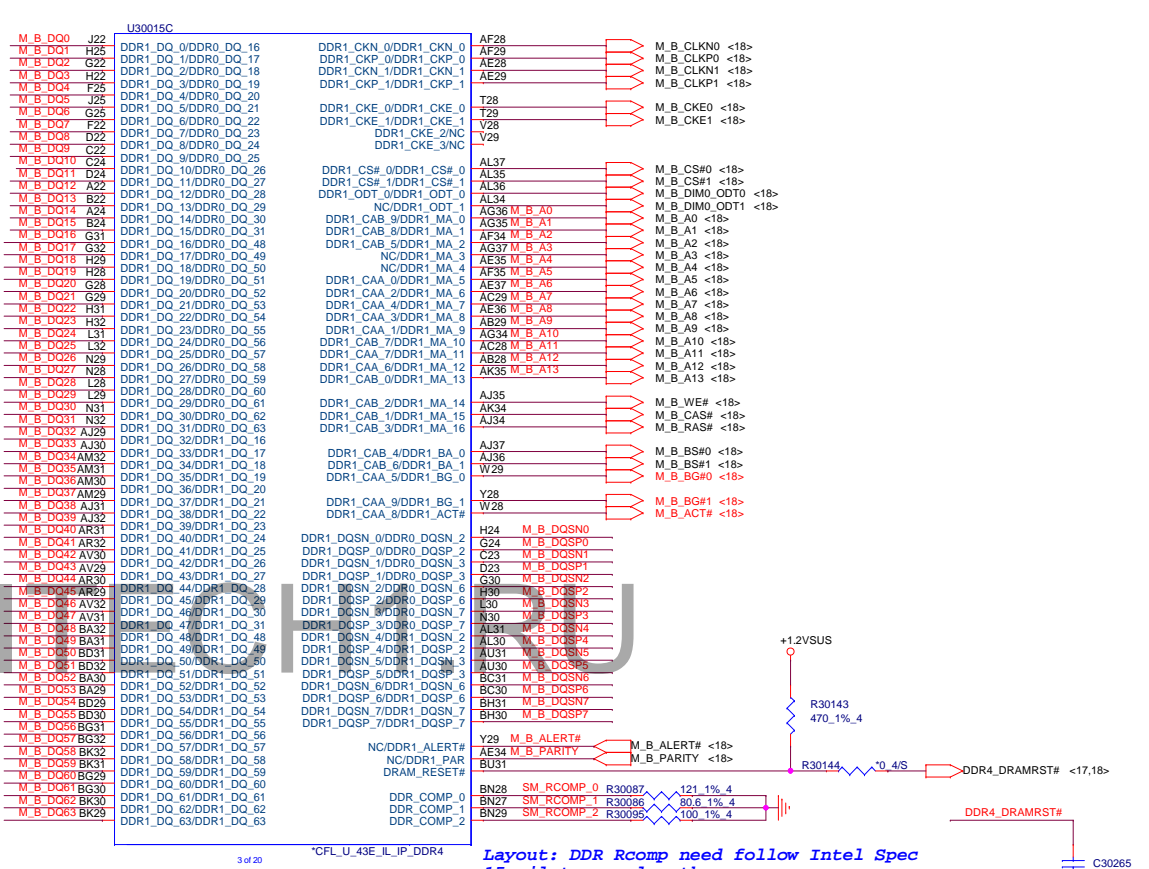
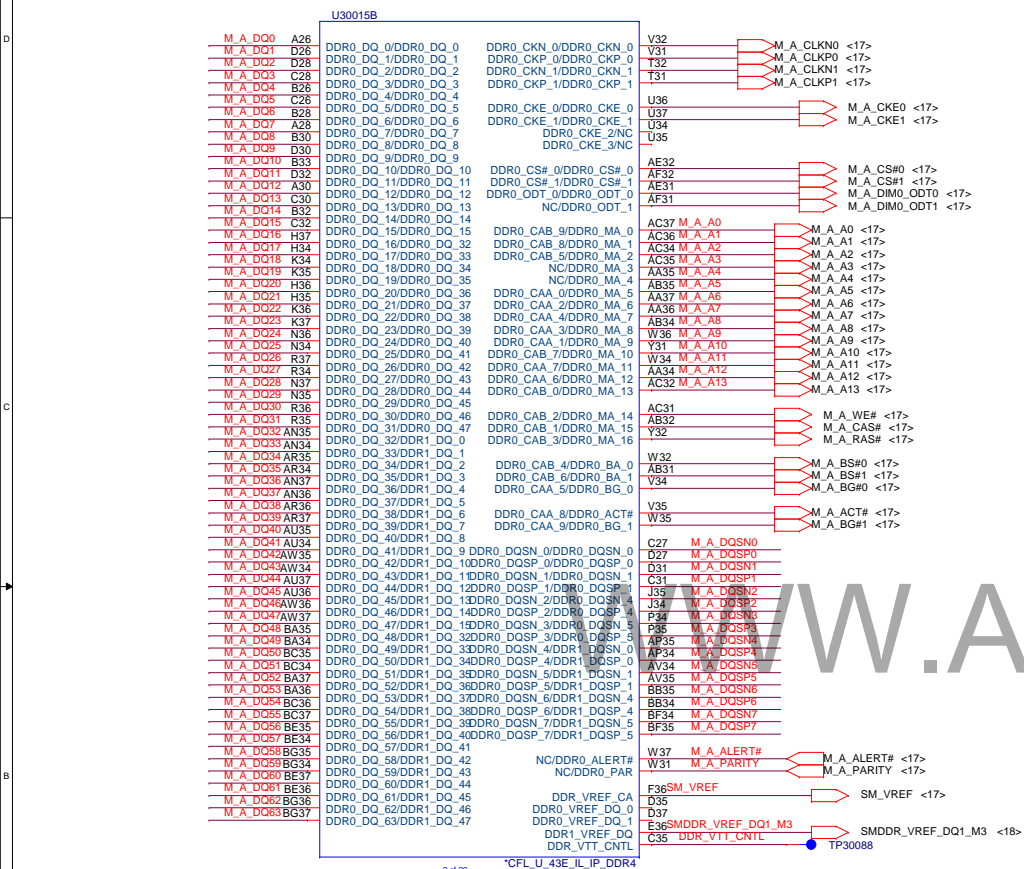
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT



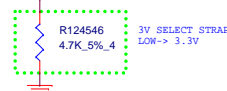
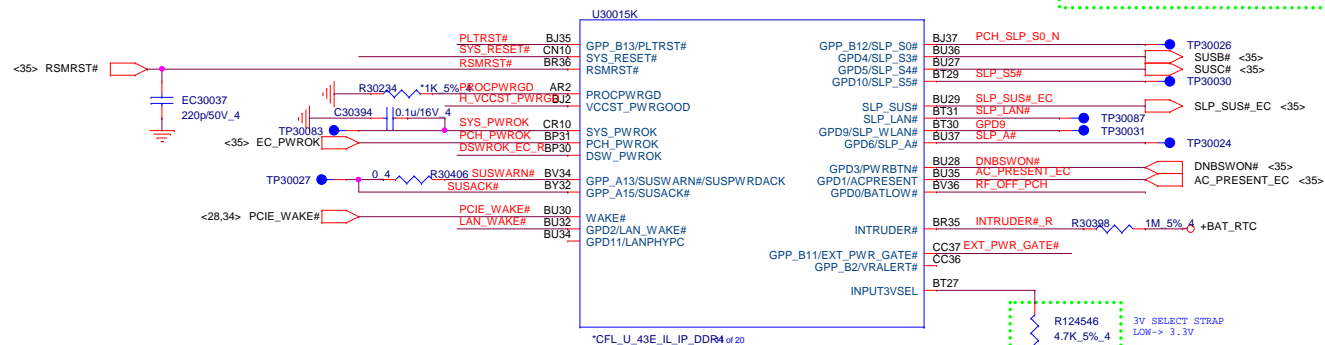
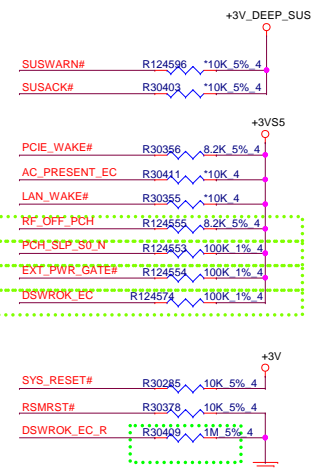
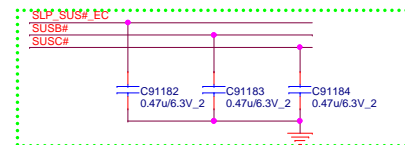
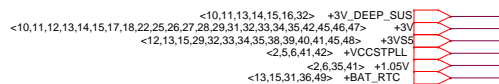


## WHL ULT Processor (MEM-A)

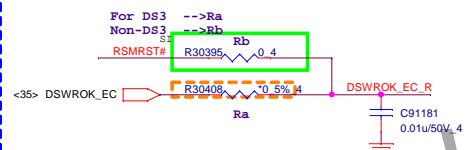
## WHL ULT Processor (MEM-B)



Layout: DDR Rcomp need follow Intel Spec  
15 mil trace length

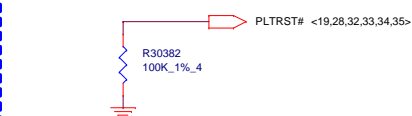


### For DS3 Sequence

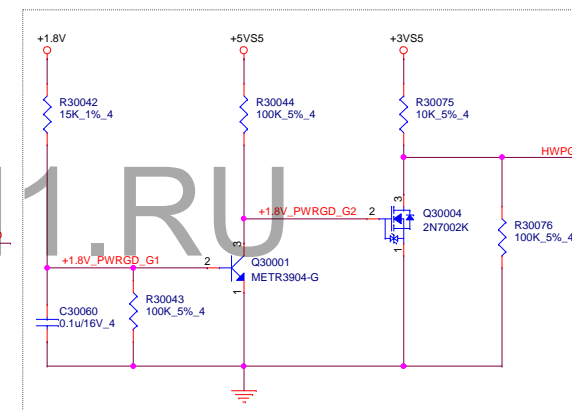
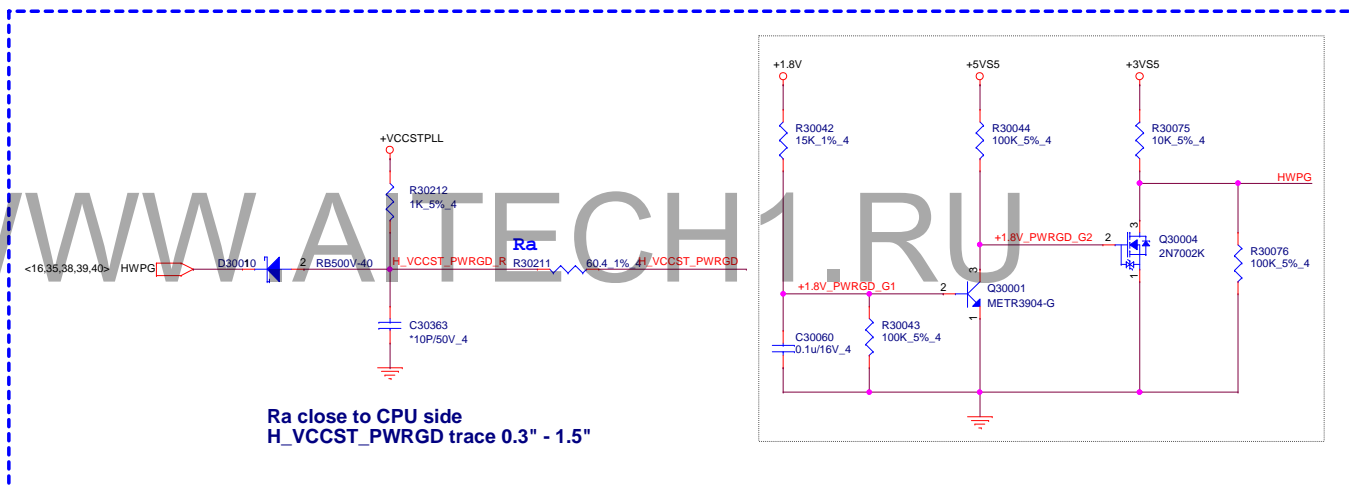
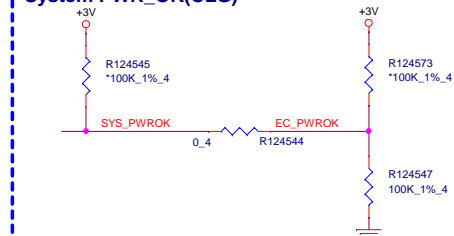


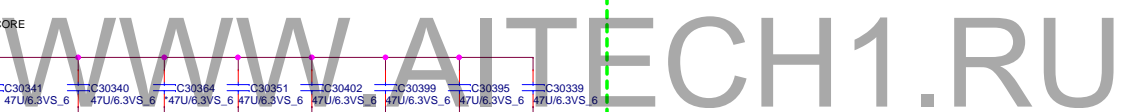
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

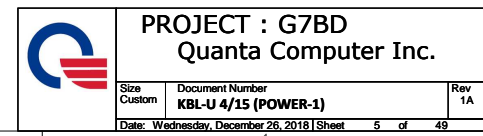


### System PWR\_OK(CLG)

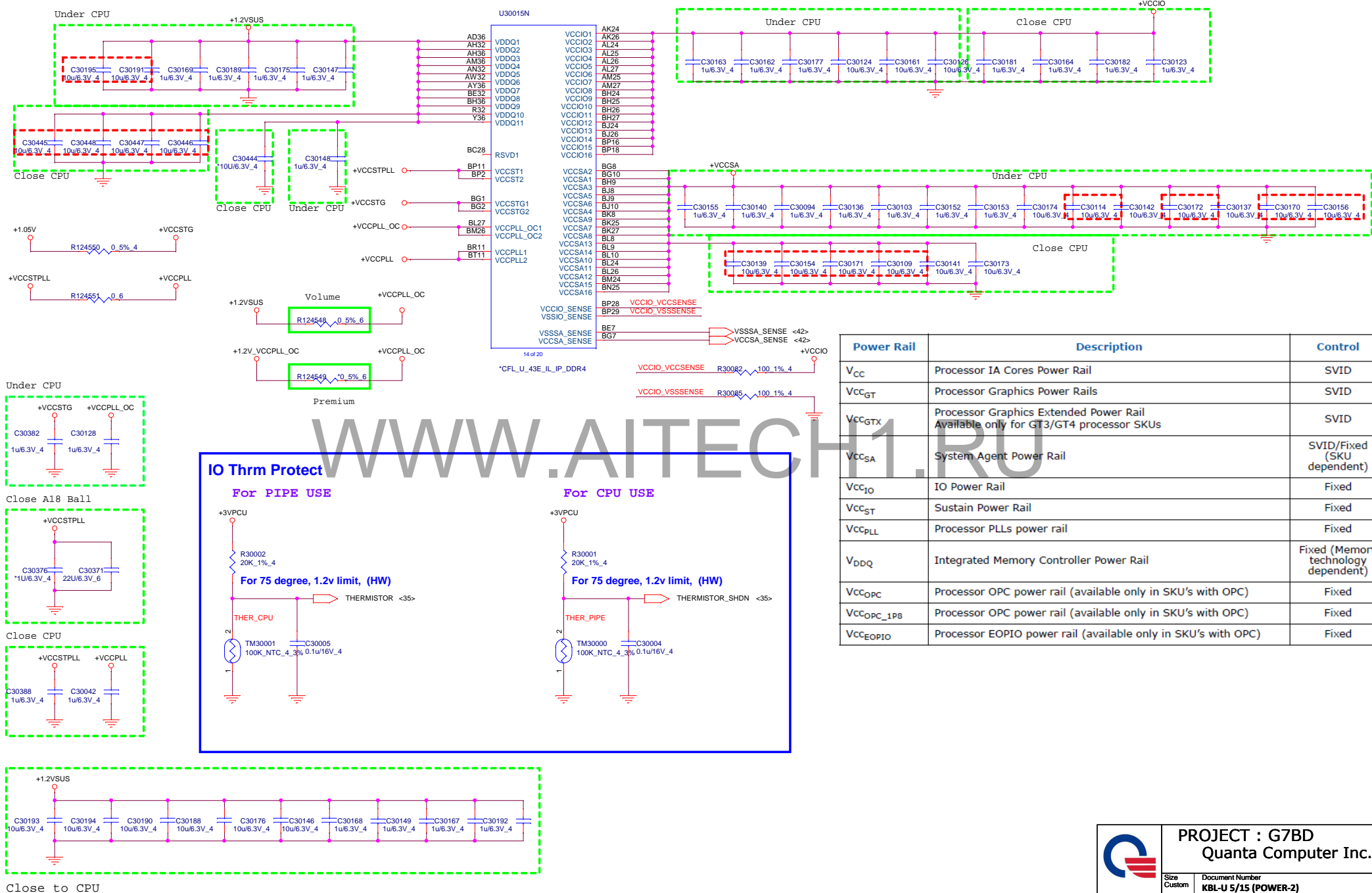




**Layout note: need routing together and ALERT need between CLK and DATA.**

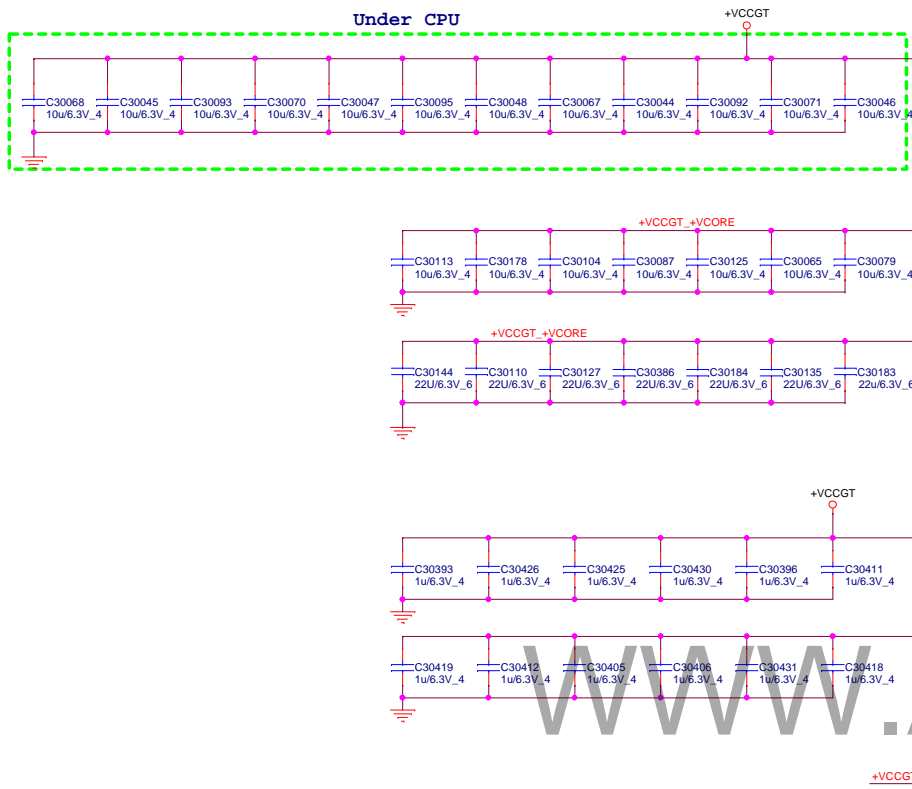


+VCCSTPLL <2.4,5,41,42>  
 +VCCSA <42,44>  
 +1.2VSUS <3,17,18,39,41>  
 +1.05V\_DEEP\_SUS <9,15,33,40,41>  
 +1.05V <2,35,41>  
 +3VPCU <13,31,34,35,36,38,49>

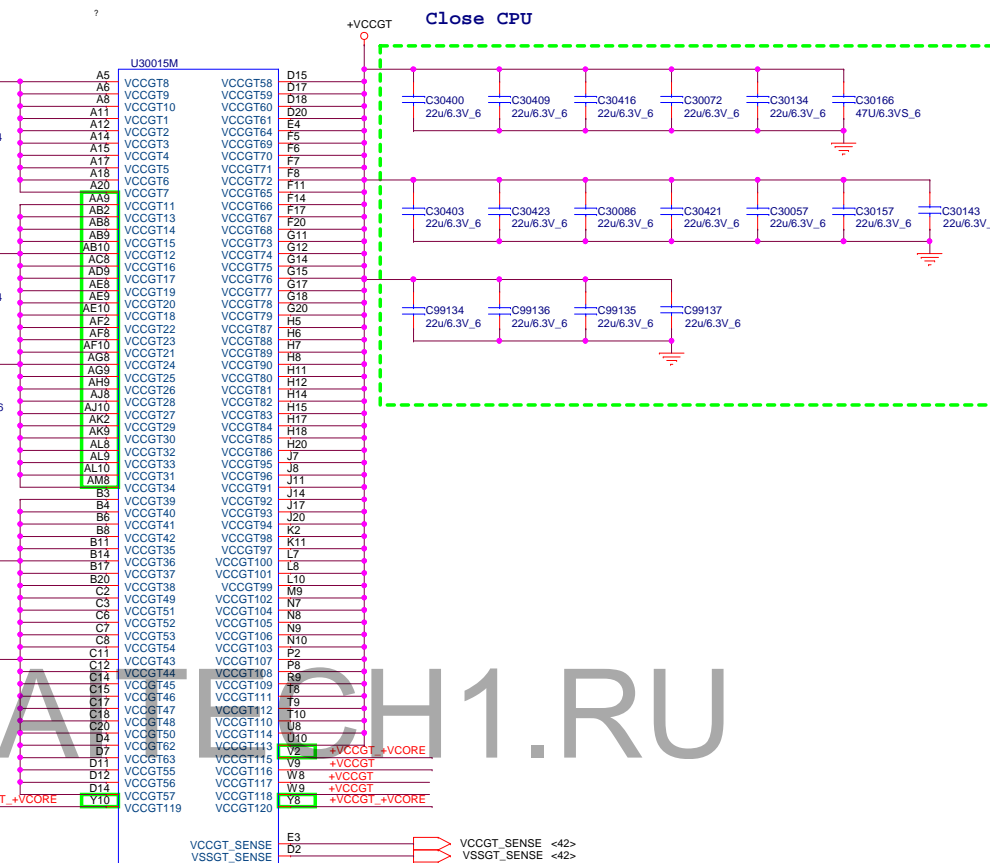


+VCCGT <42,44>  
+VCC\_CORE <45,42,43>  
+1.2VSUS <3,6,17,18,39,41>

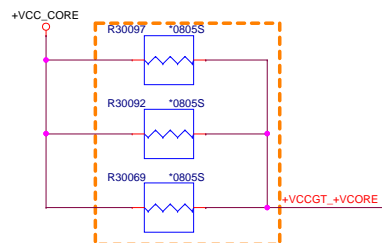
## Under CPU



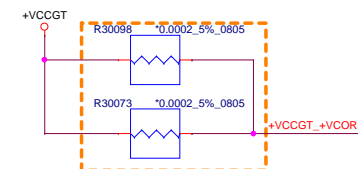
## Close CPU



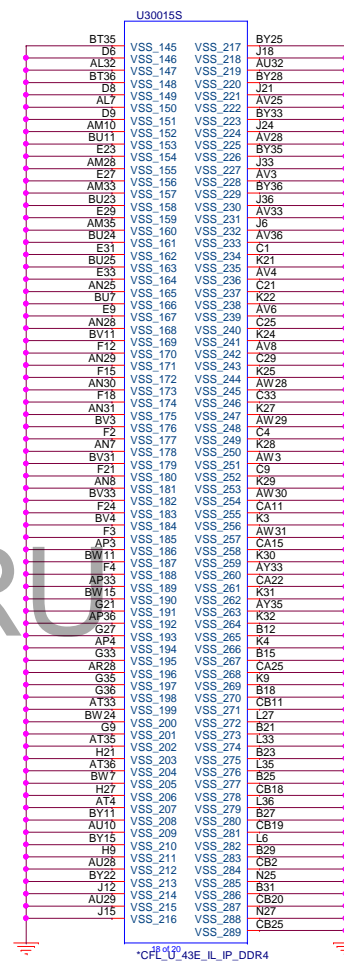
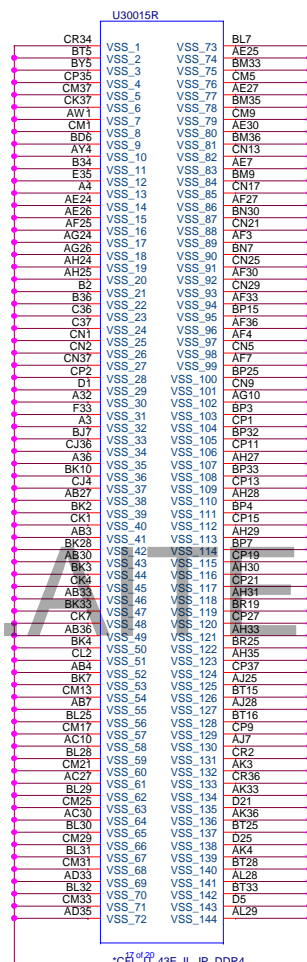
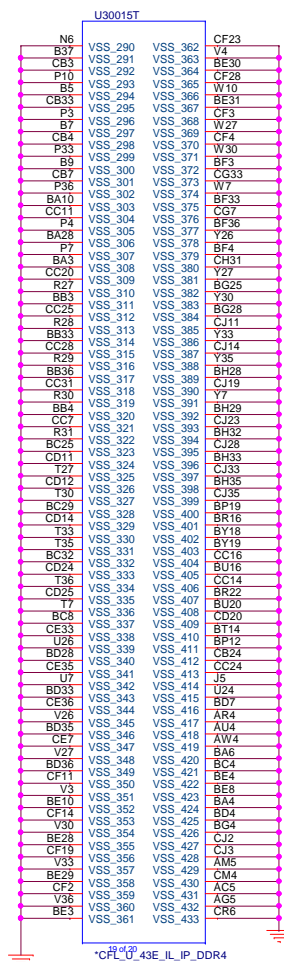
Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

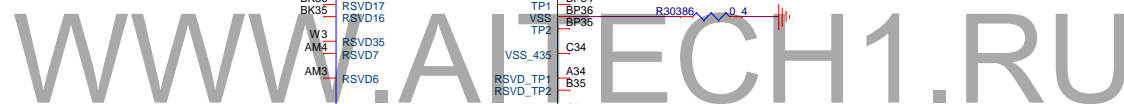


For WHL U42 ES2 上件/0122



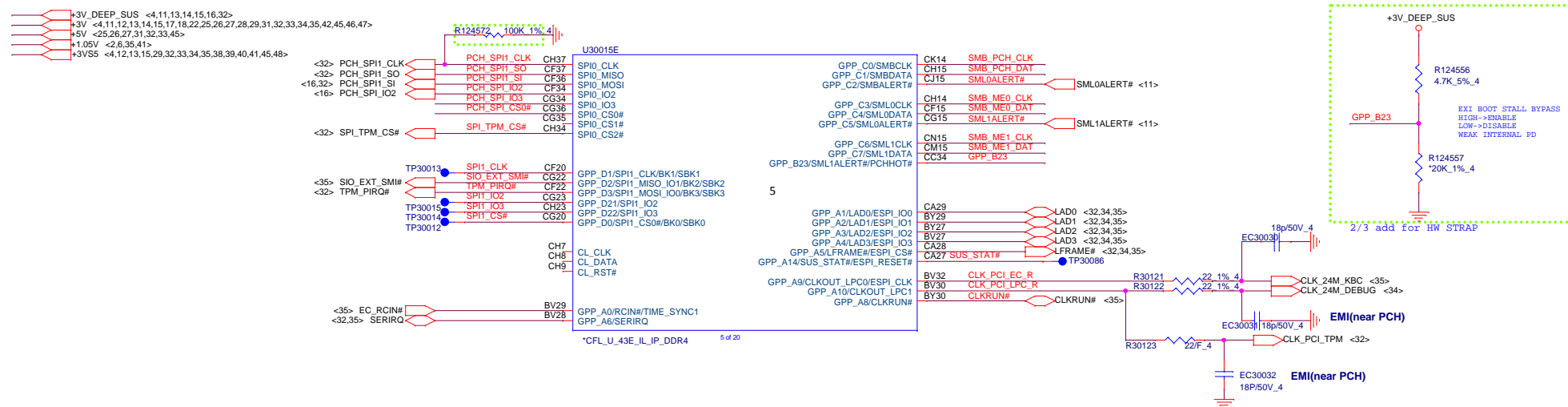
For WHL U42 ES1 上件/0122



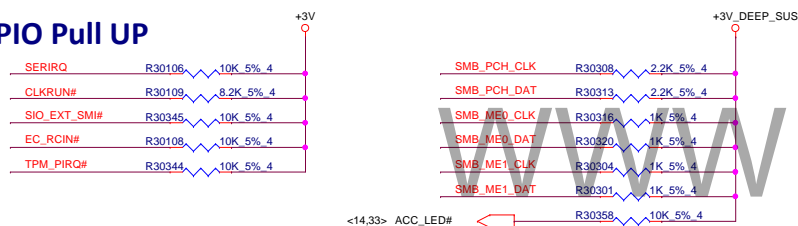


	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	





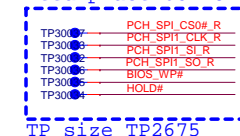
## GPIO Pull UP



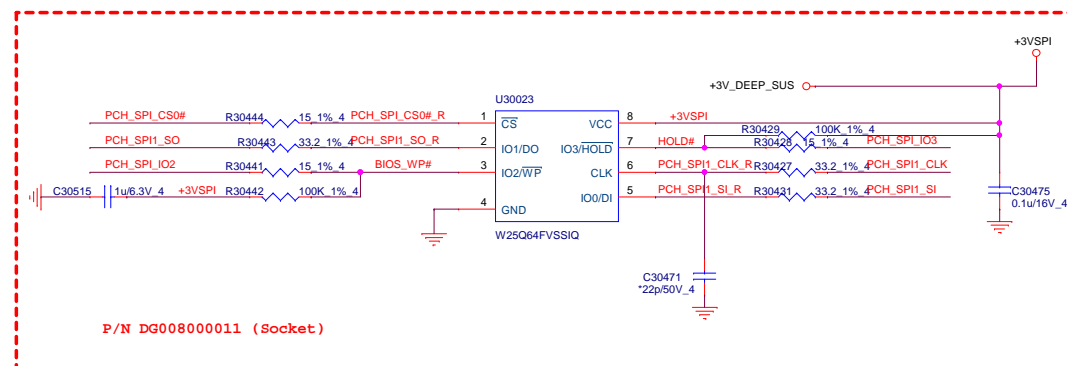
## PCH SPI ROM(CLG)

Vender	Size	P/N
MXIC	16MB	AKE3DZN0Z03 (MX25L12873FM2I-10G)
Winbond	16MB	AKE3DF-KN01 (W25Q128JVSIG)
GigaDevice	16MB	AKE3DZN0Q02 (GD25B127DSIGR)
Socket		DG008000011

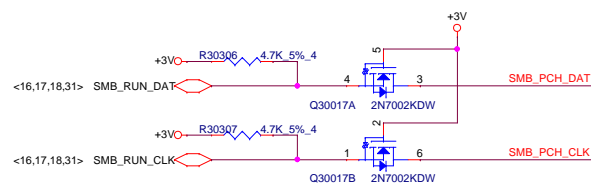
need place to TOP



## PCH SPI ROM(CLG)

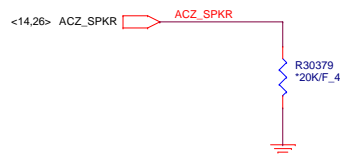


P/N DG008000011 (Socket)

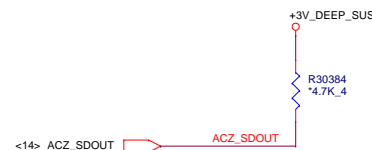
CPU heat pipe local thermal sensor  
DDR thermal sensor  
ECTouch Pad  
XDP  
DDR4

# Functional Strap Definitions

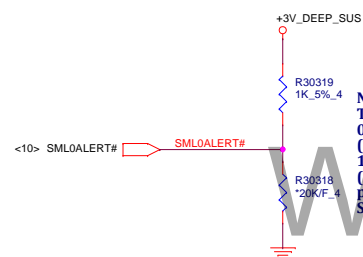
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



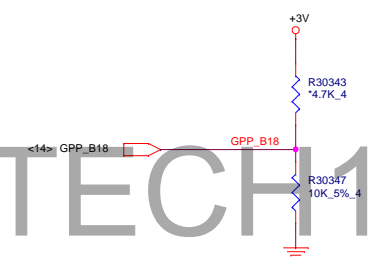
**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD



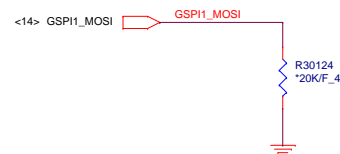
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



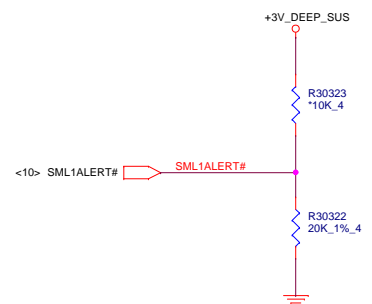
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



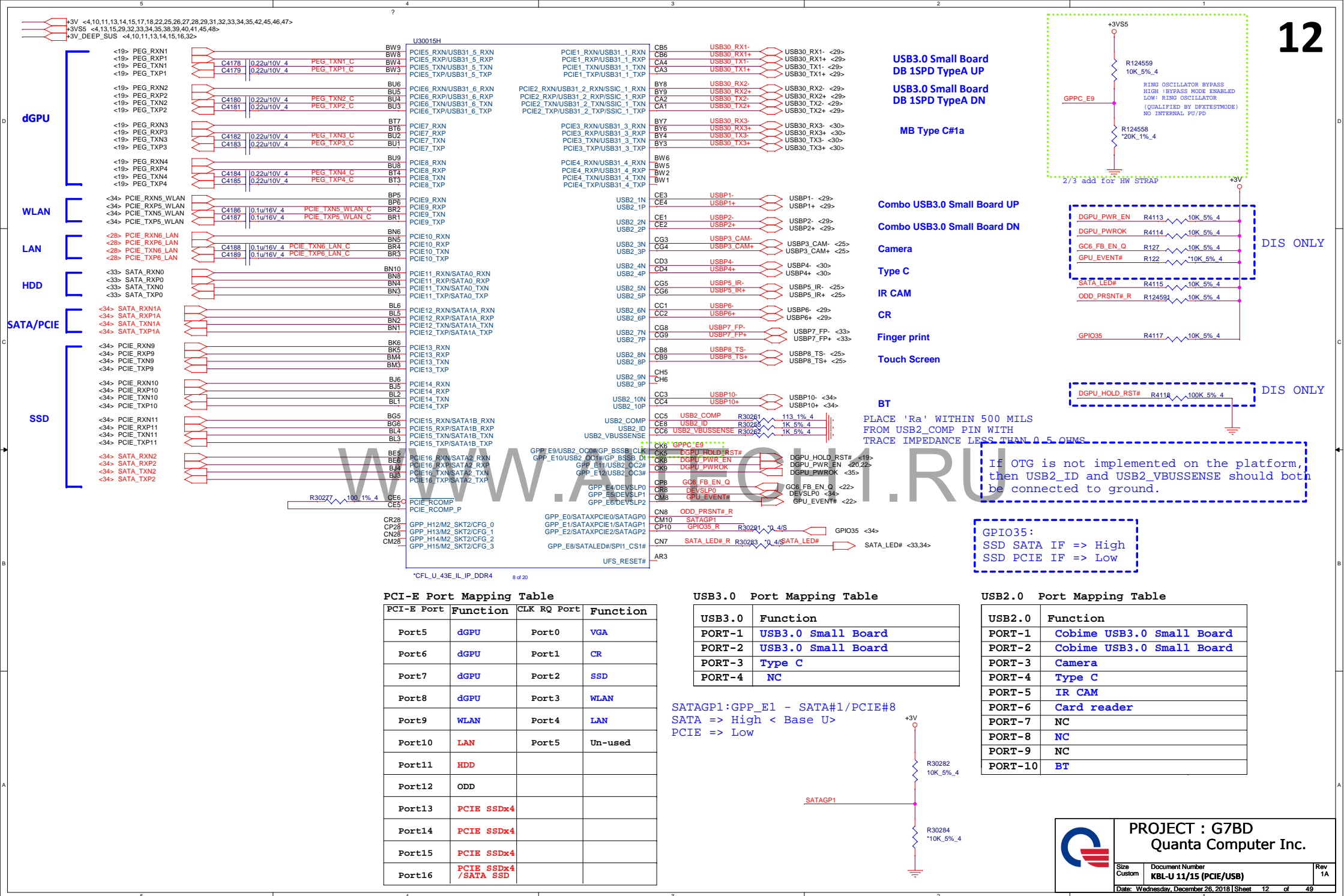
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

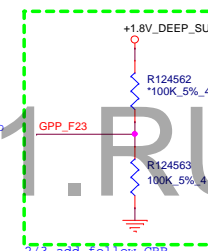
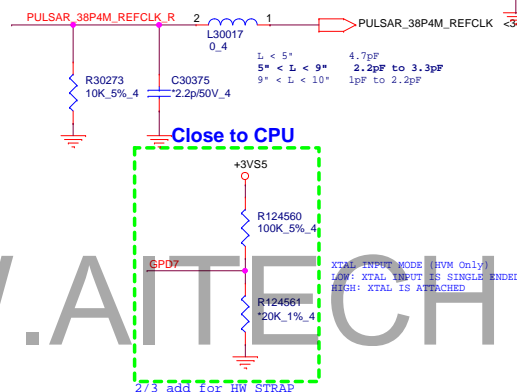
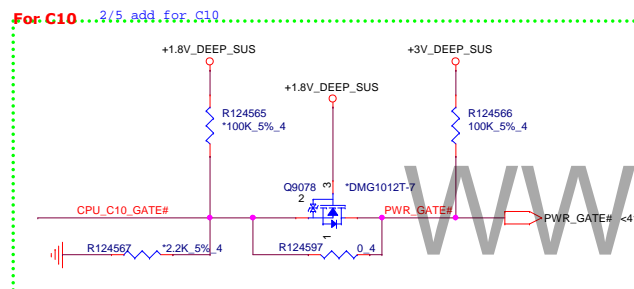
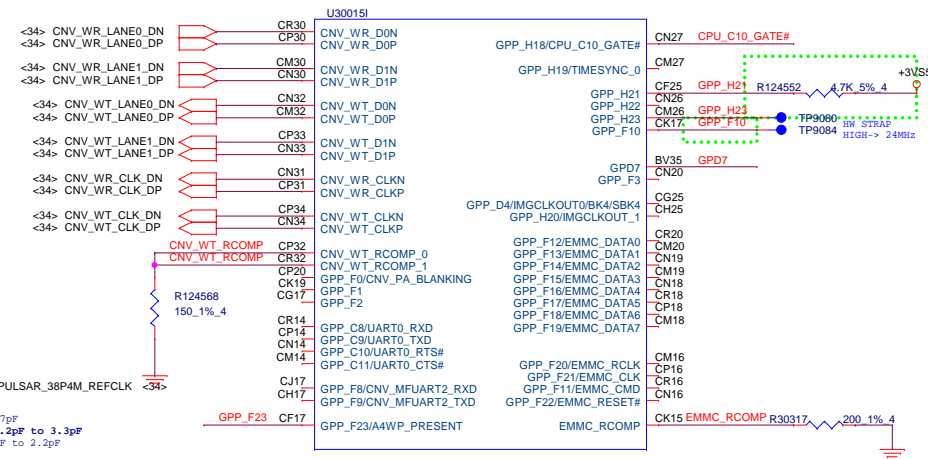


**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10      Boot BIOS Destination**  
0            SPI  
1            LPC



**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



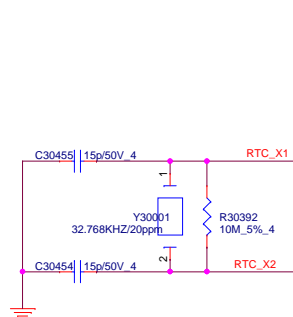


### CLK\_REQ/Strap Pin(CLG)

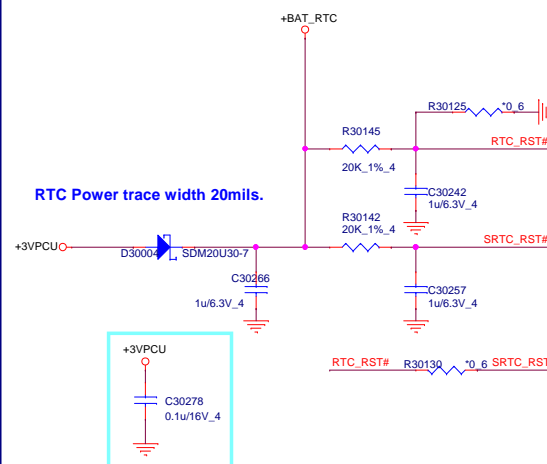


## RTC Circuitry(RTC)

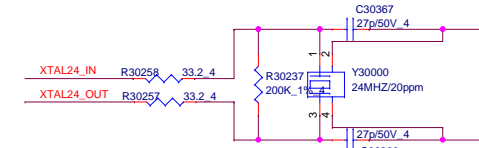
30mils



RTC Power trace width 20mils.



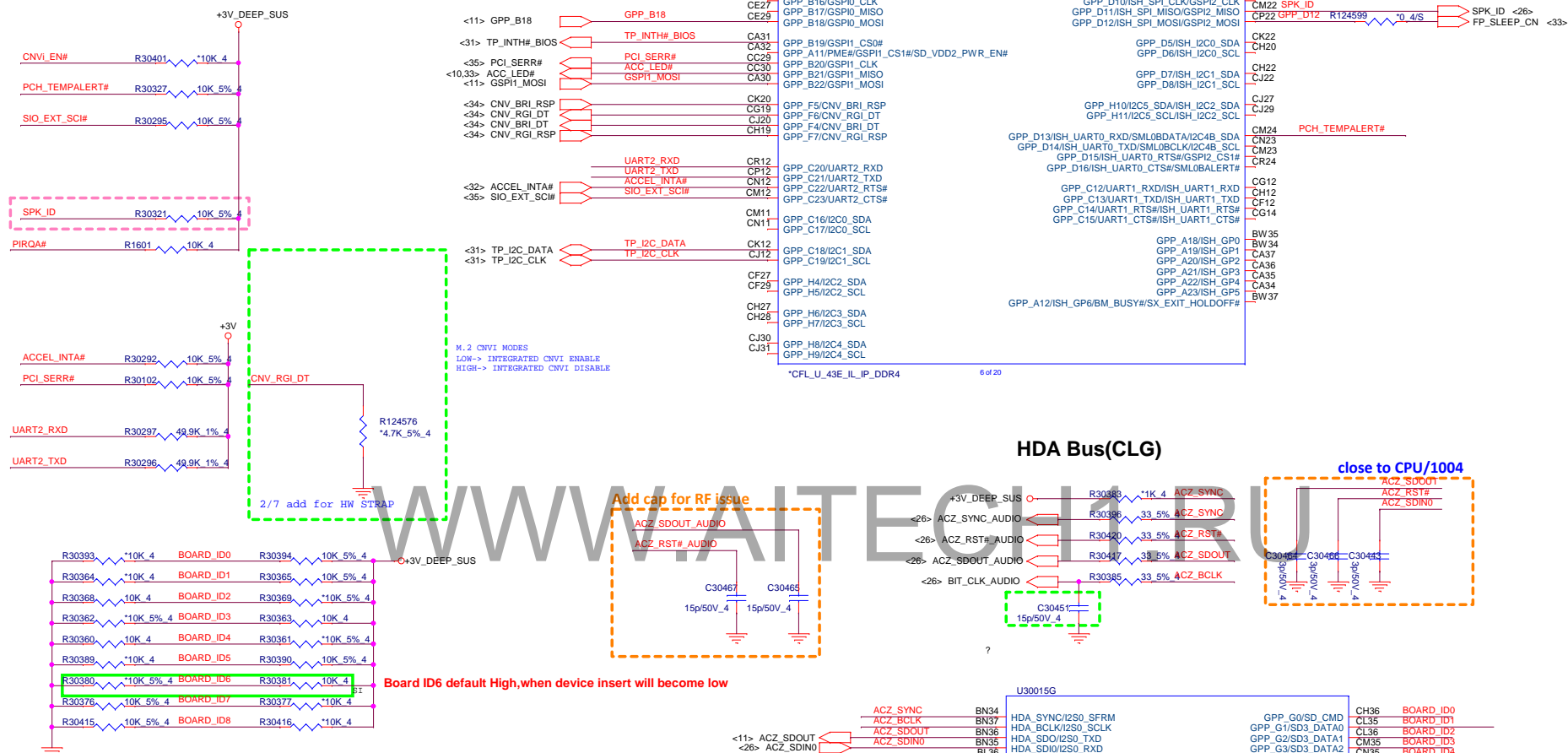
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



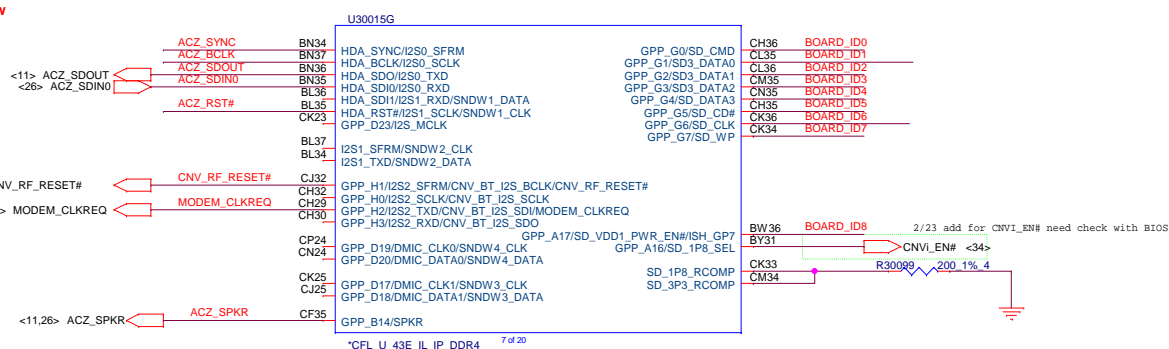
PROJECT : G7BD Quanta Computer Inc.
--

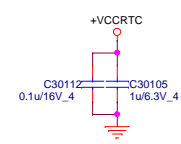
Size Custom	Document Number <b>KBL-U 12/15 (CLK/EMMC)</b>	Rev 1A
Date: Wednesday, December 26, 2018   Sheet 13 of 49		

## WHLake (GPIO)



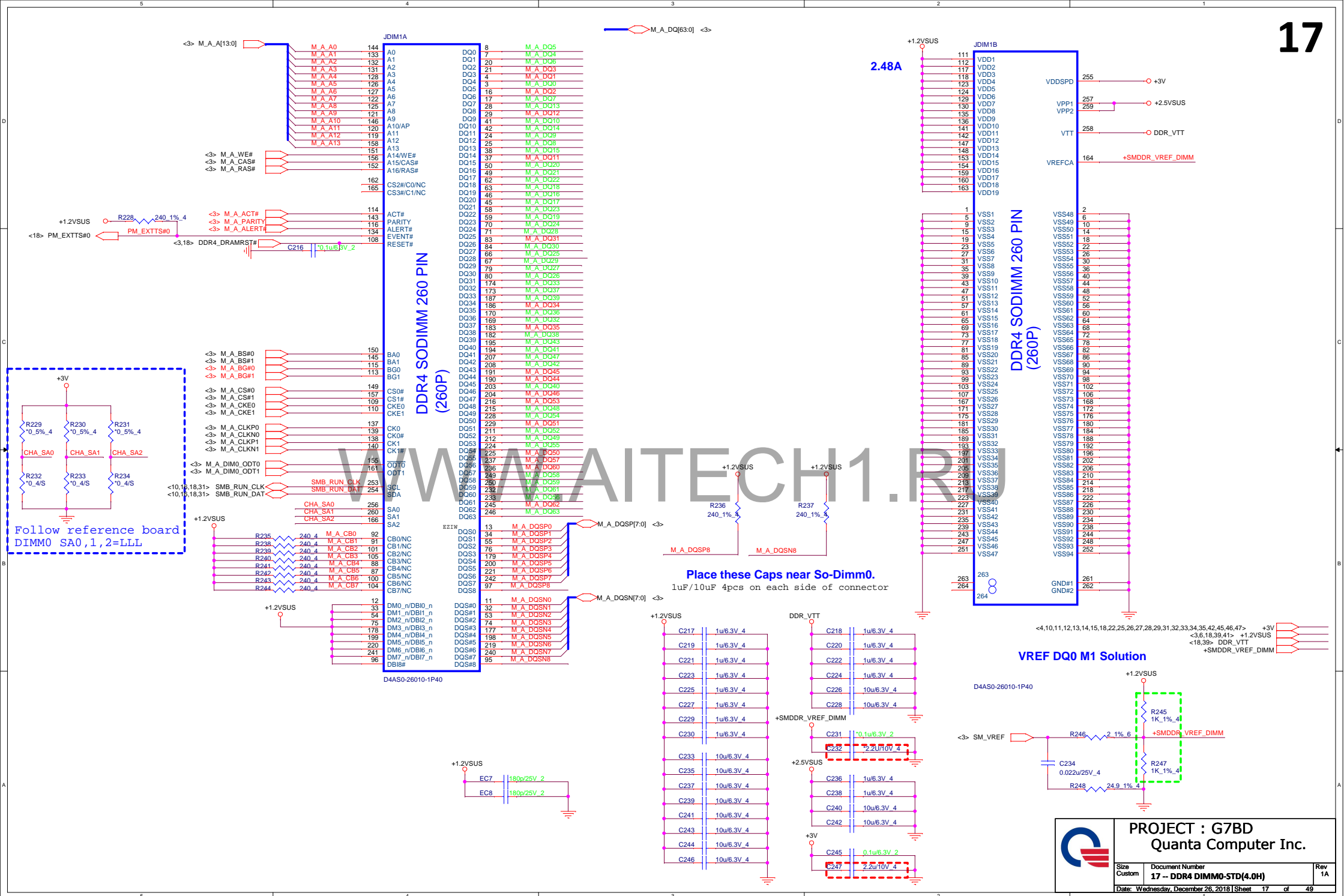
WHL	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	BOARD_ID[3:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3 ID2 ID1	ID0
Definition	Reserve (Default = 00)	0: Finger Print 1: Non-Finger Print	0 : AMD 1 : Nvidia GPU setting	0 : 2G VRAM 1 : 4G VRAM	100 : 14" (WHL) 000 : 14" 110 : 2SPD (WHL) 010 : MAX-Q 111 : 13" (WHL) 011 : 2SPD	0 : UMA 1 : DIS

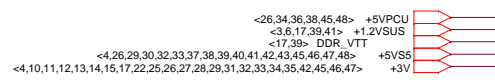


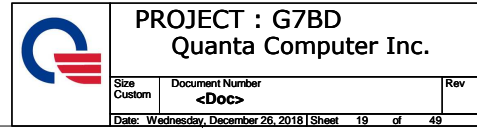




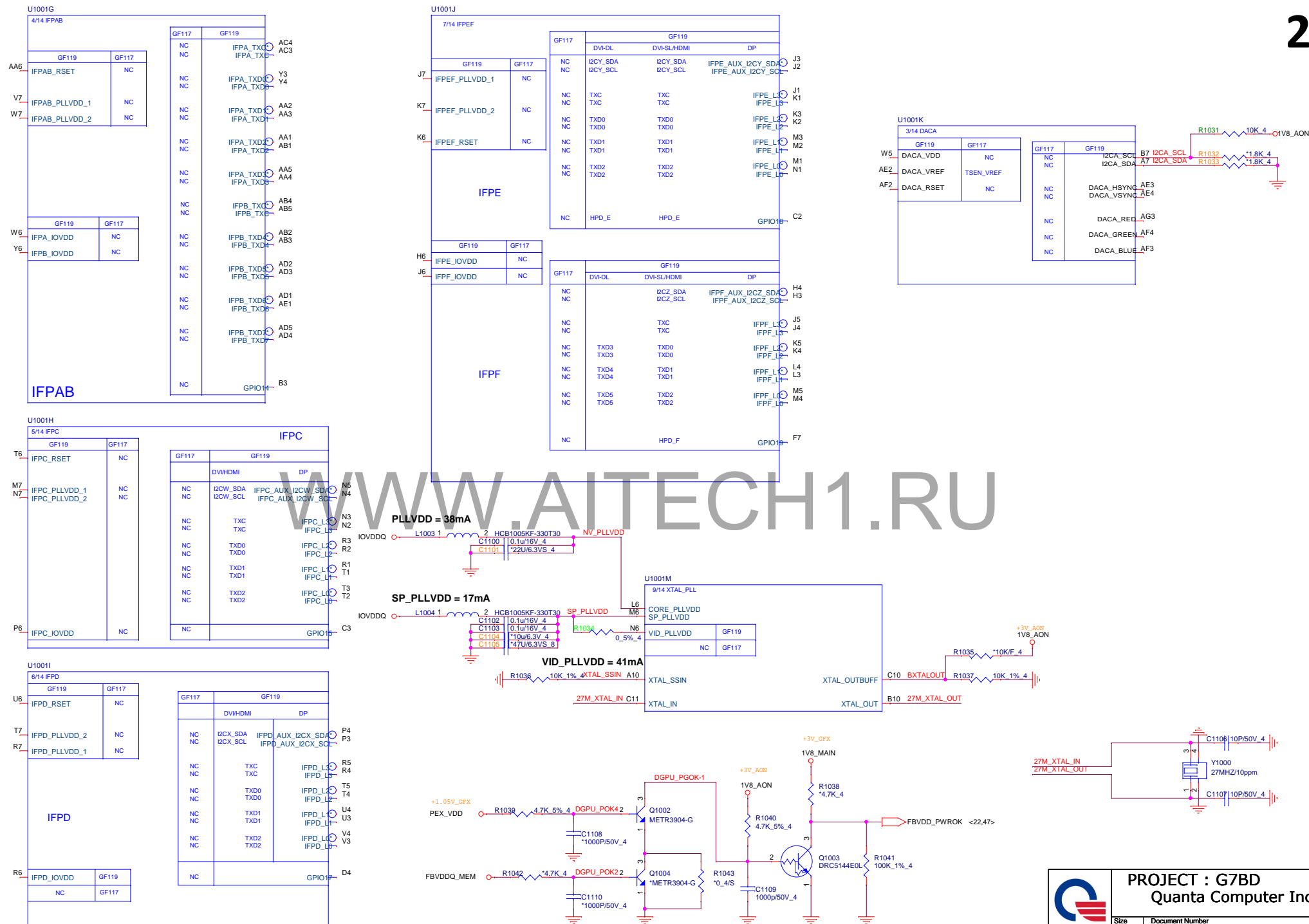
WWW.AITECH1.RU















<b>N16S strap setting</b>	
ROM_SI	VRAM Configuration follow VRAM table
ROM_SD	Stuff 4.98V Pull Up CS14492P25
ROM_SCLK	Stuff 4.98V Pull Down CS14492P25
STRAP0	Stuff 49.9K Pull Up CS14492P10
STRAP1	NC
STRAP2	NC
STRAP3	NC
STRAP4	NC
STRAP5	NC

<b>N17S strap setting</b>	
ROM_SI	Stuff 100K Pull Up CS41002P20
ROM_SD	Stuff 100K Pull Up CS41002P20
ROM_SCLK	Stuff 100K Pull Up and 100K Pull Down CS41002P20
STRAP0	VRAM Configuration follow VRAM table
STRAP1	VRAM Configuration follow VRAM table
STRAP2	VRAM Configuration follow VRAM table
STRAP3	Stuff 100K Pull Down CS41002P20
STRAP4	Stuff 100K Pull Down CS41002P20
STRAP5	Stuff 100K Pull Down CS41002P20

	STRAP2	STRAP1	STRAP0	
Samsung	L	L	L	0x0000
Micron	H	L	L	0x0004
Hynix	H	L	H	0x0005

STRAP[2:0] VRAM Table for N17S-G1 GDDR5 Recommended Memories

BANK# [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	AKG5QGD1509	AKG5QGD1508
0x4	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x5	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

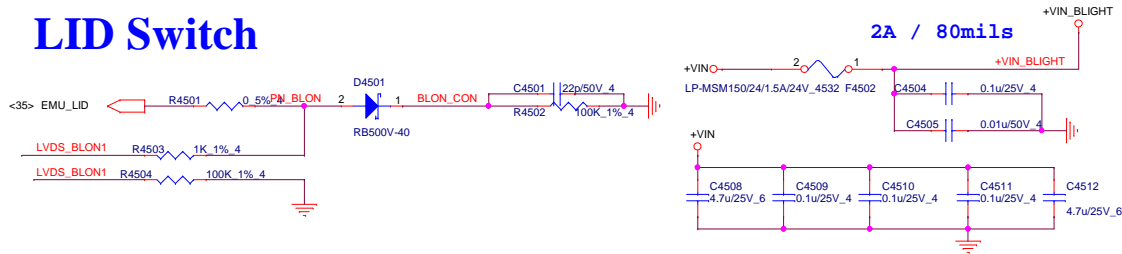
ROM SI VRAM Table for N16S-GTR GDDR5 Recommended Memories

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N
0x0	GDDR5 512Mx16 7 GHz	Samsung B die	K4G80325FB-BC28	AKG5QGD1509	AKG5QGD1508
0x8	GDDR5 512Mx16 8 GHz	Micron B die	MT51J256M32HF-80:B	AKG5QGUTL24	AKG5QGUTL25
0x9	GDDR5 512Mx16 8 GHz	Hynix A die	H5GC8H24AJR-R2C	AKG5QGUTW15	AKG5QGUTW16

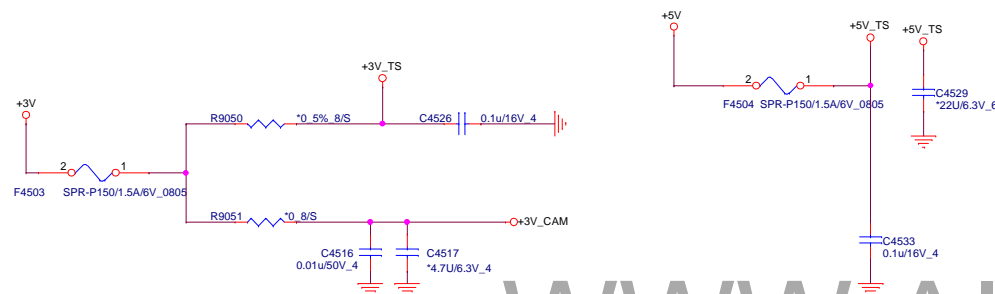
R1055	SAMSUNG	6000	4.98V	CS24992P25
R1046	HYUNIX	1001	4.98V	CS11002P25

WWW.AITECH1.RU

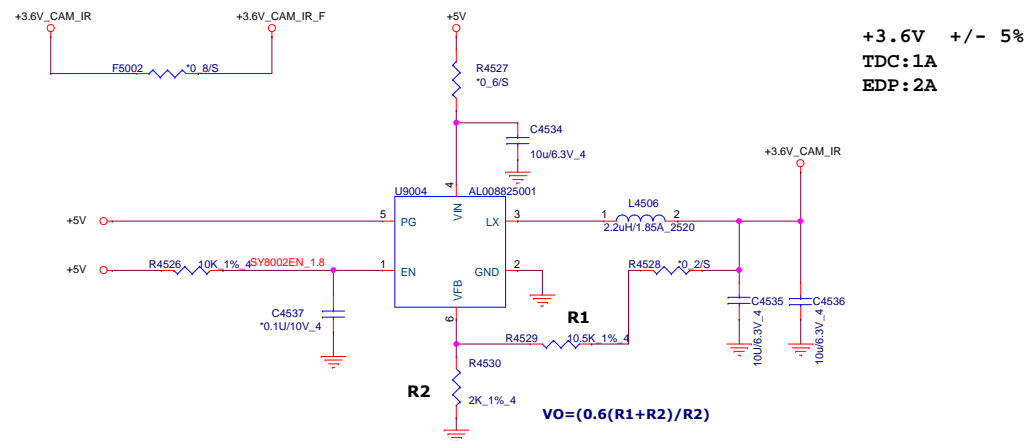
## LID Switch



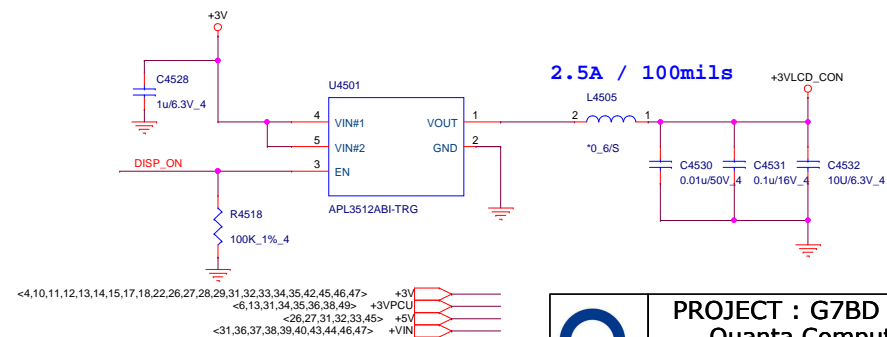
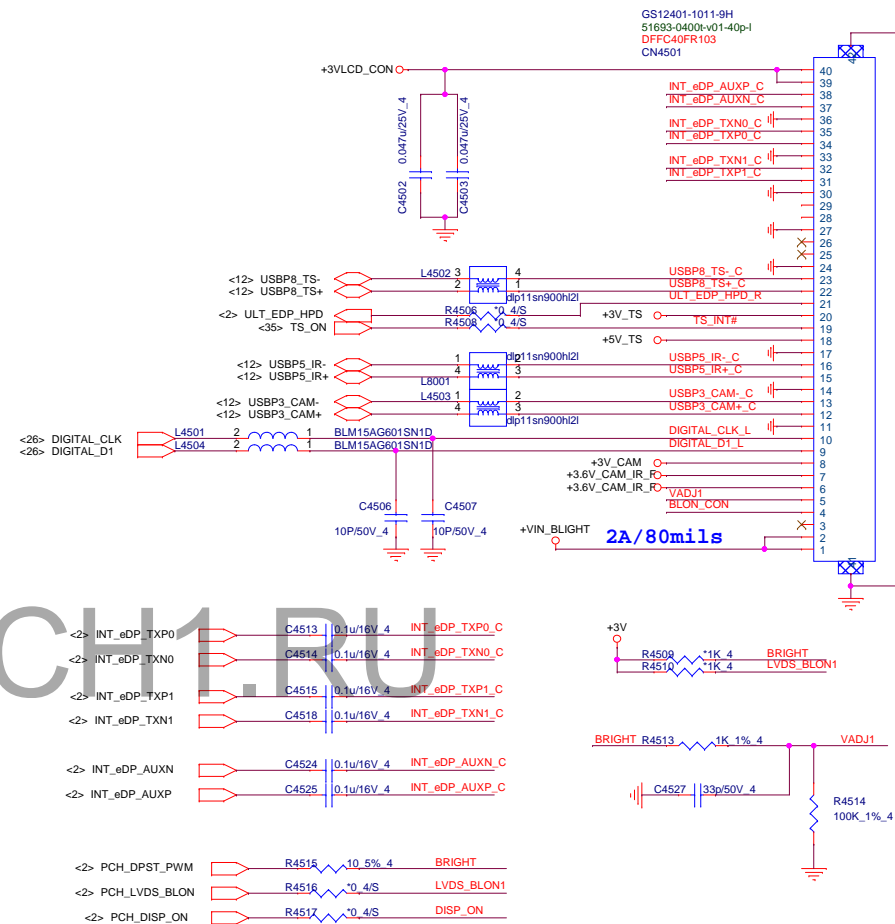
## Touch screen

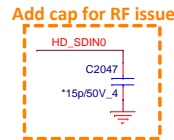
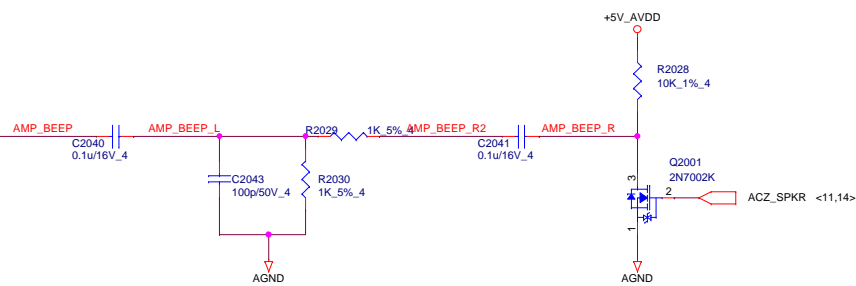
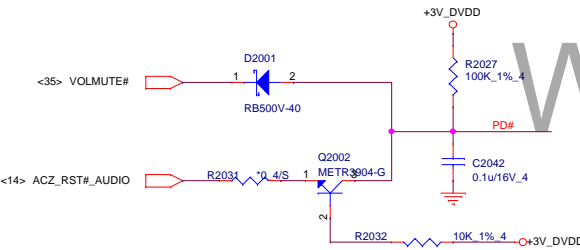
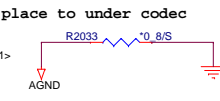
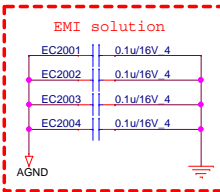
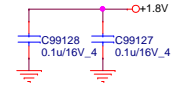
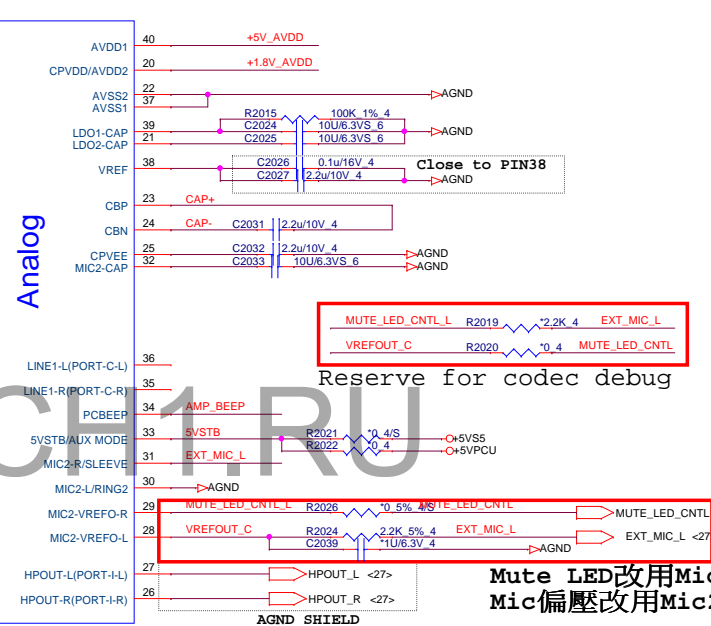
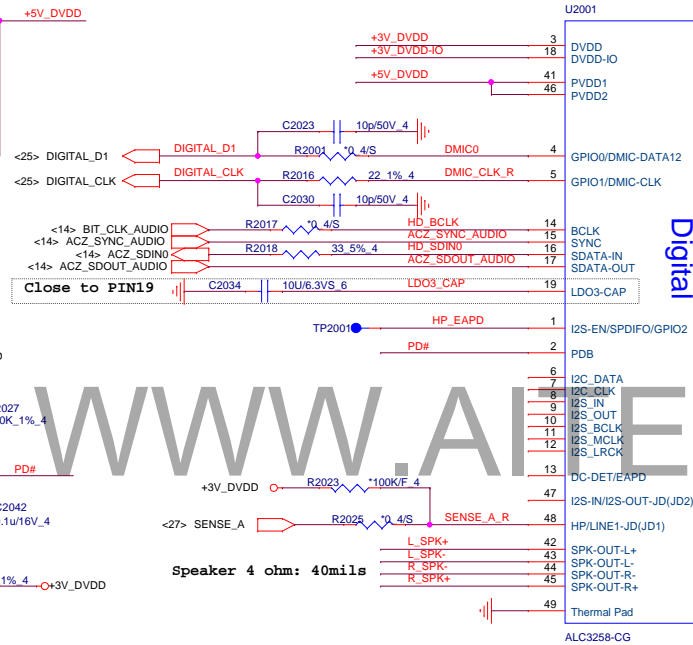
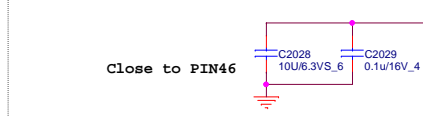
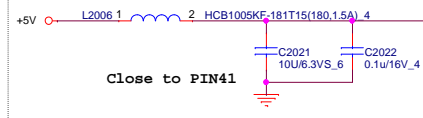
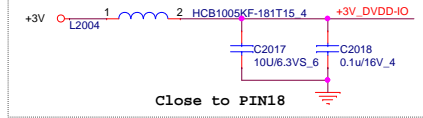
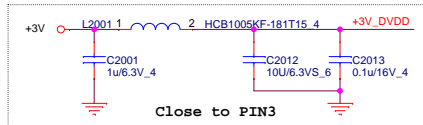


## IR CAM

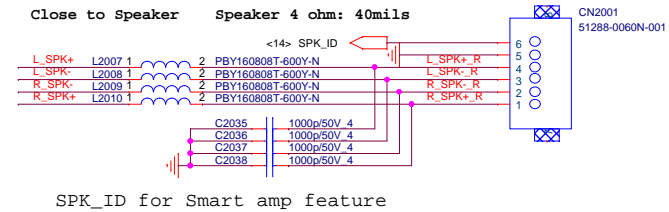


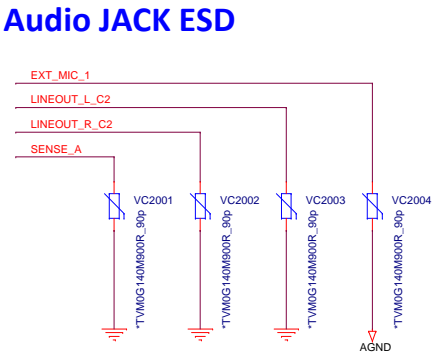
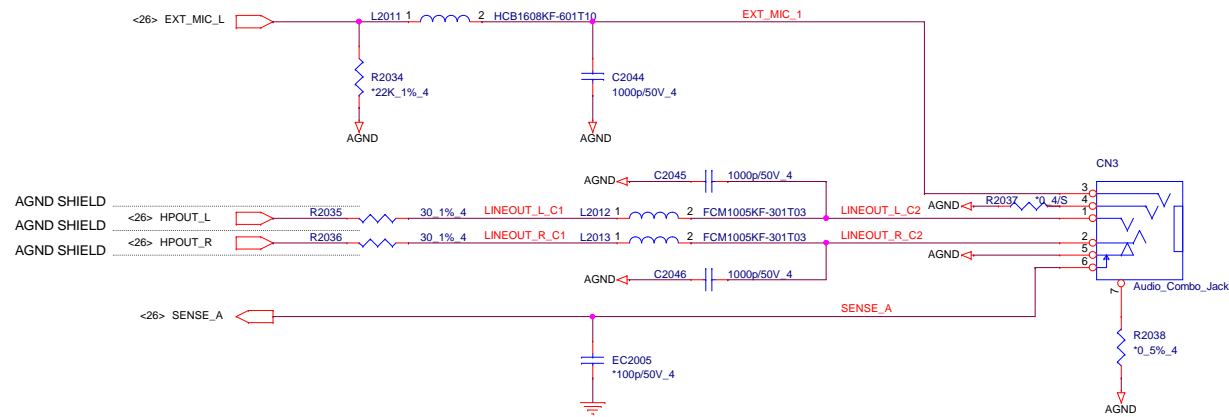
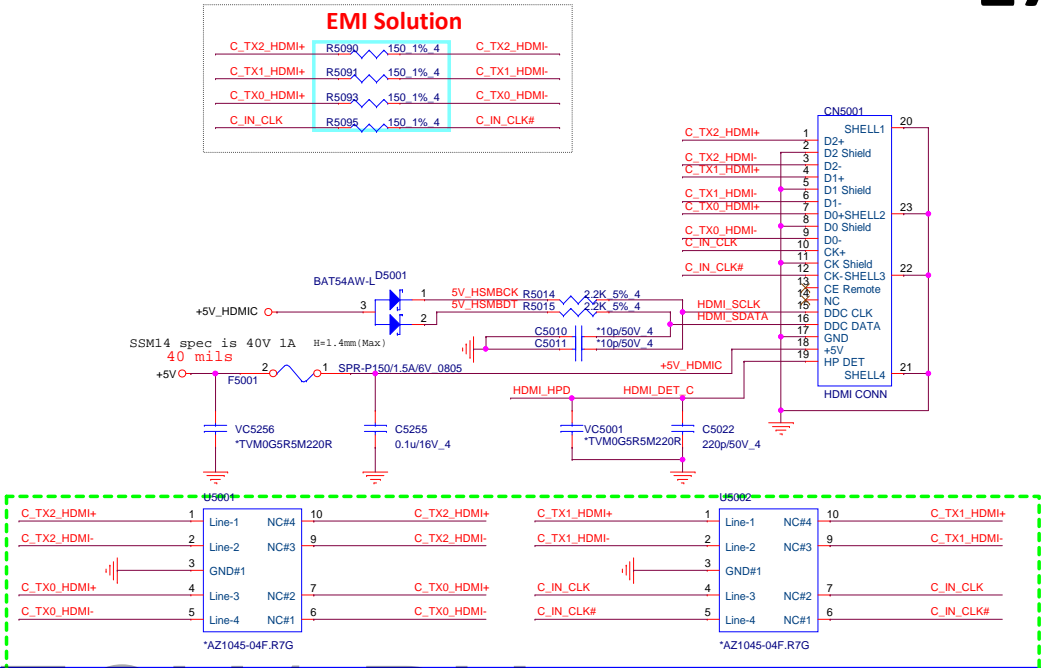
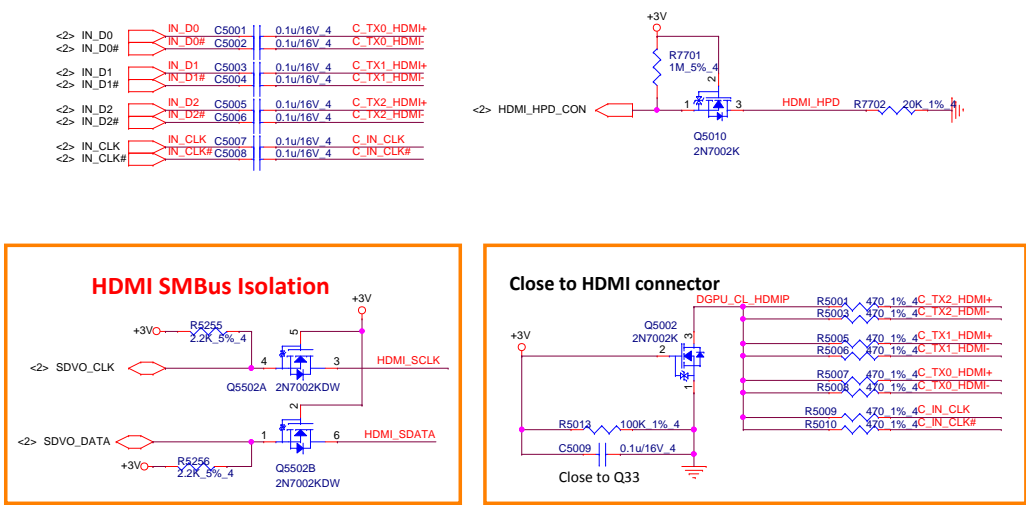
## eDP Conn.





## SPK CONN





# LAN RTL8111HSH-CG

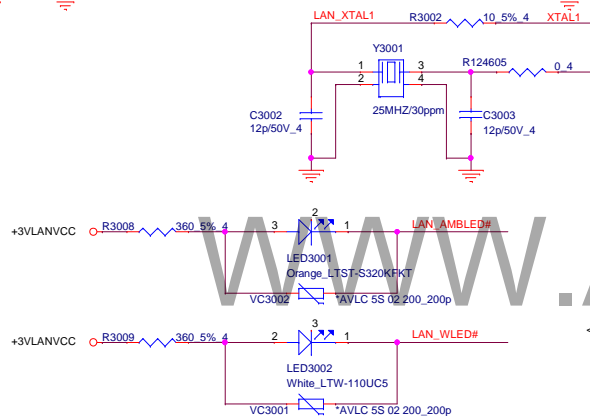
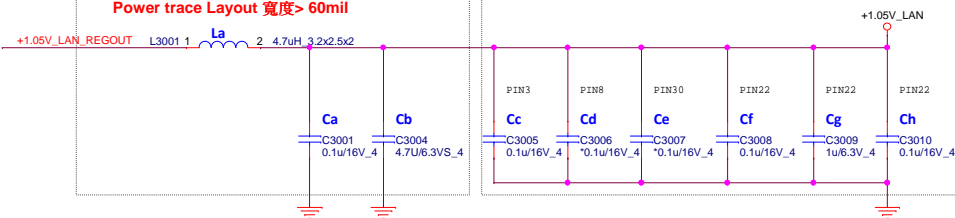
28

For SWR mode support  
RTL8107ESH-CG/RTL8111HSH-CG  
Stuff: La, Ca, Cb

\* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG  
close to each VDD10 pin-- 3, 22, 8, 30

\* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG  
close to each VDD10 pin-- 22(reserved)

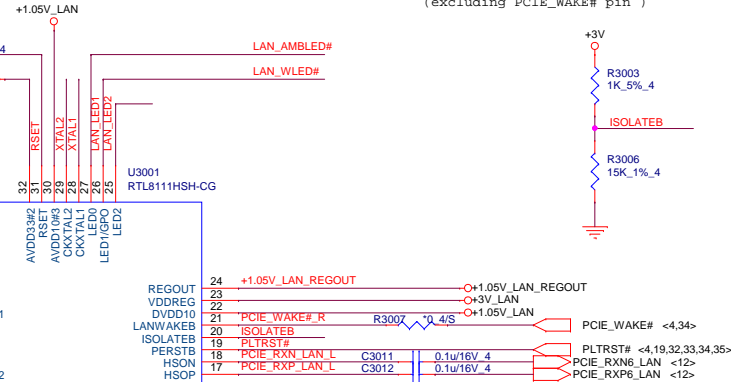
Power trace Layout 宽度> 60mil



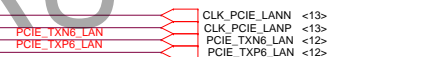
Add 9 GND VIAs with thermal PAD



if ISOLATEB pin pull-low,  
the LAN chip will not drive it's PCI-E outputs  
(excluding PCIE\_WAKE# pin)

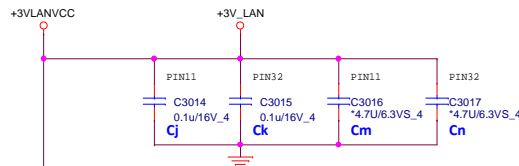


For GbE  
\* Place RTL8111HSH-CG AL008111014  
For 10/100  
\* Place RTL8107ESH-CG AL008107000

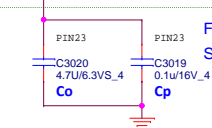


\* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for  
RTL8107ESH-CG/RTL8111HSH-CG

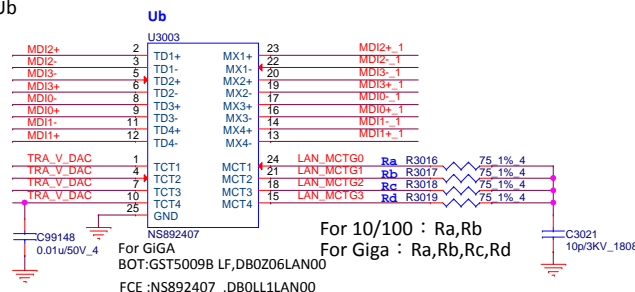
\* For surge improvement, place Cm and Cn, close to each  
VDD33 pin-- 11, 32(optional)



For SWR mode support RTL8107ESH-CG/RTL8111HSH-CG  
Stuff Co, Cp

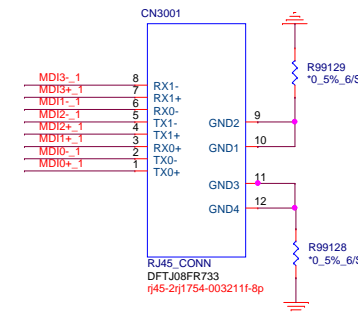


For Giga : Ub



For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd

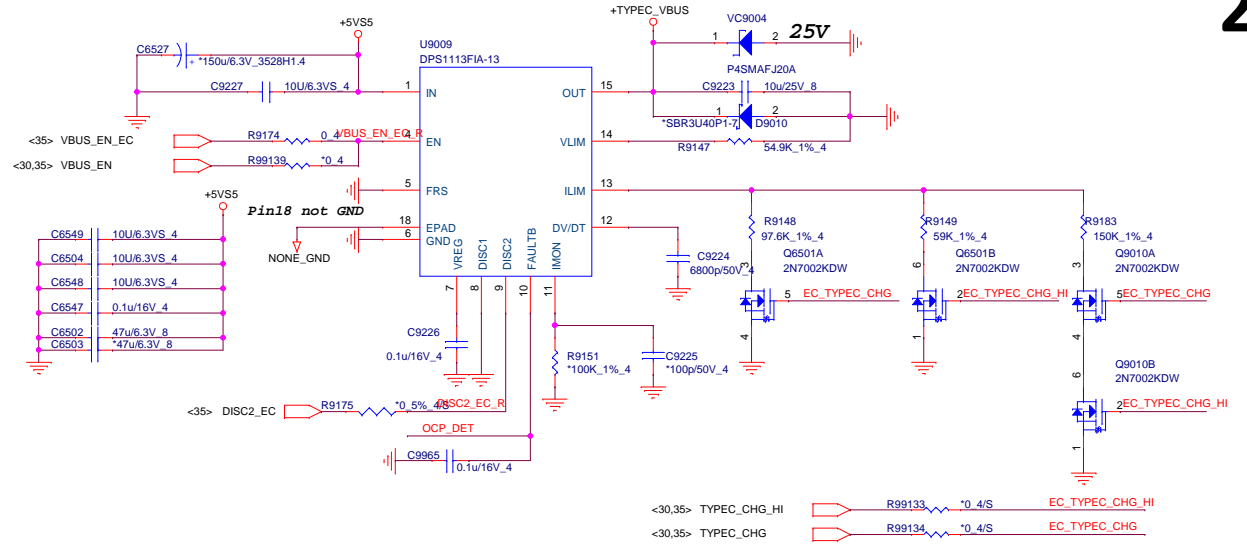
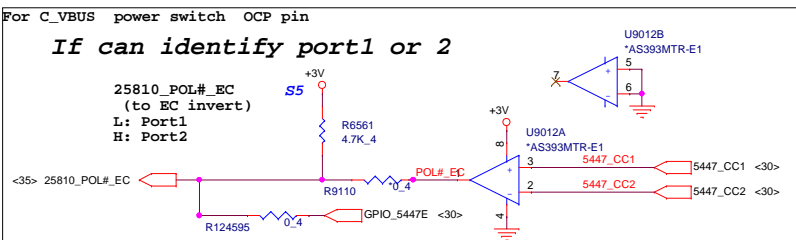
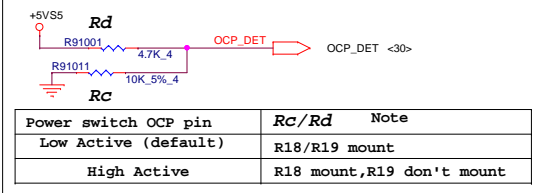
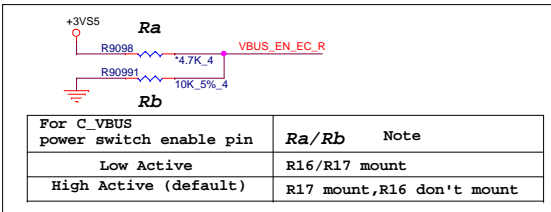
RJ45



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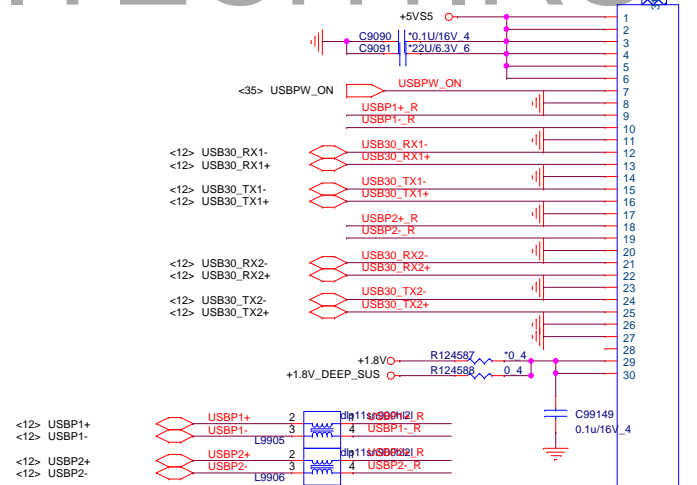
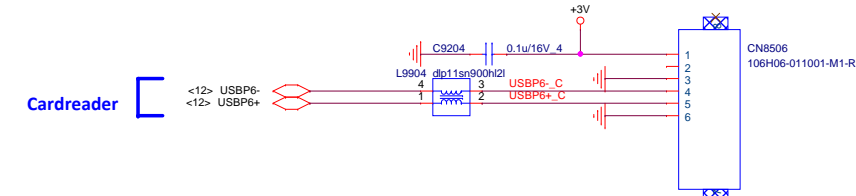
# USB TYPEC POWER SWITCH

29



## SD Board

## USB Board



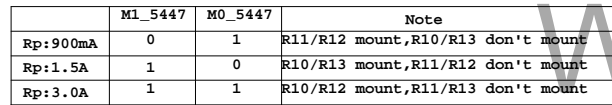
CN5502

DFFC30FR148

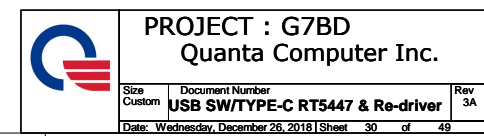
51519-03001-V01-30p-I

51519-0300T-V01

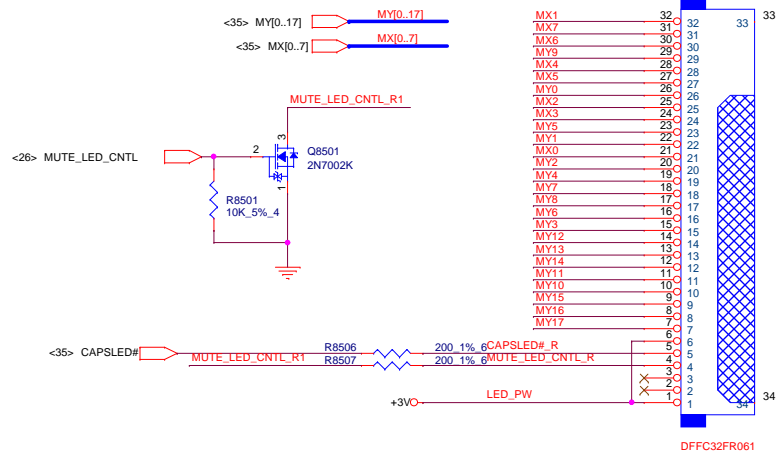
<4,26,29,32,33,37,38,39,40,41,42,43,45,46,47,48>	+5VS5		<b>30</b>
<4,12,13,15,29,32,33,34,35,38,39,40,41,45,48>	+3VS5		
<4,10,11,12,13,14,15,17,18,22,25,26,27,28,29,31,32,33,34,35,42,45,46,47>	+3V		
<29>	+TYPEC_VBUS		



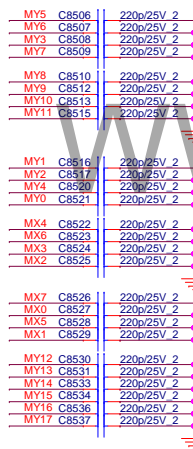
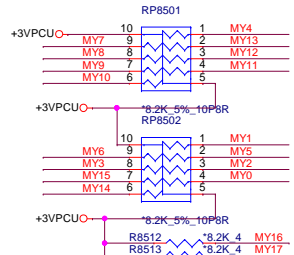
## TYPE C USB2.0 ESD



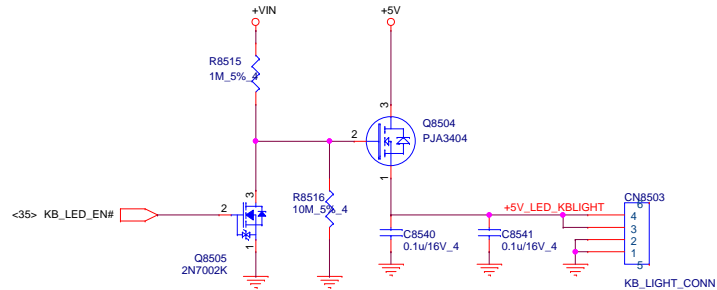
## KEYBOARD Con.



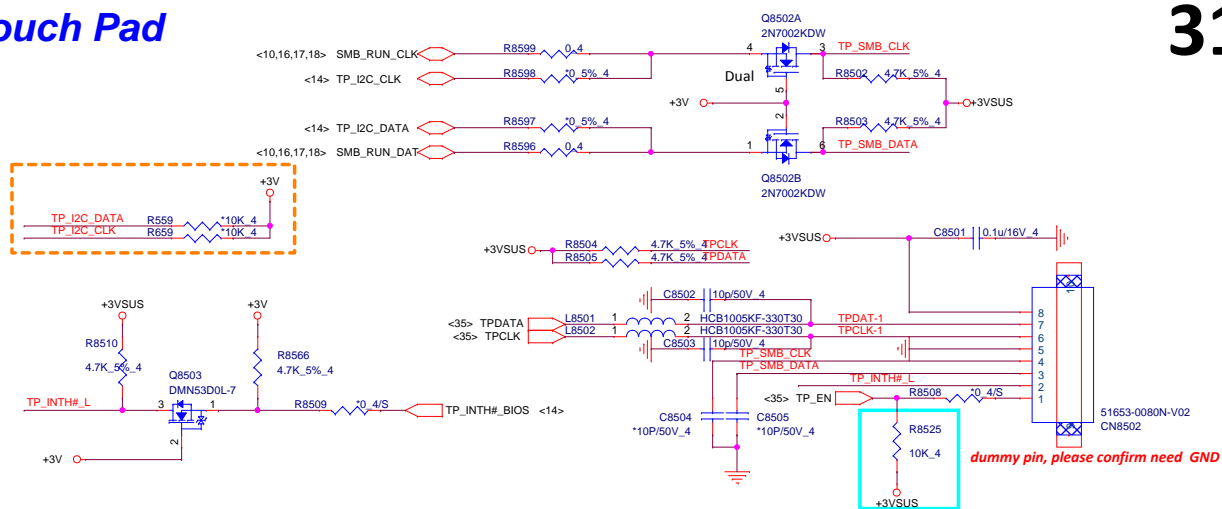
## KEYBOARD PULL-UP



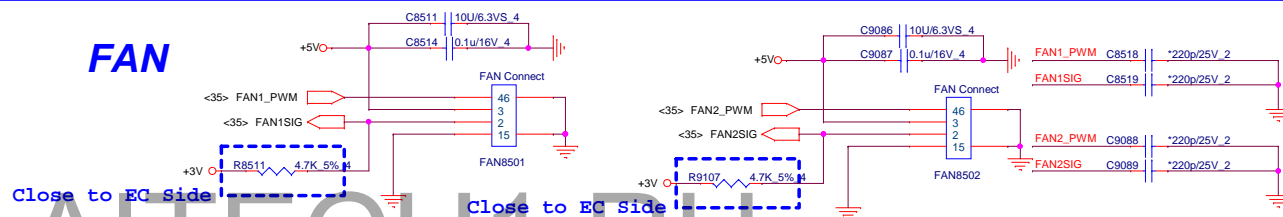
## KB LIGHT CONN



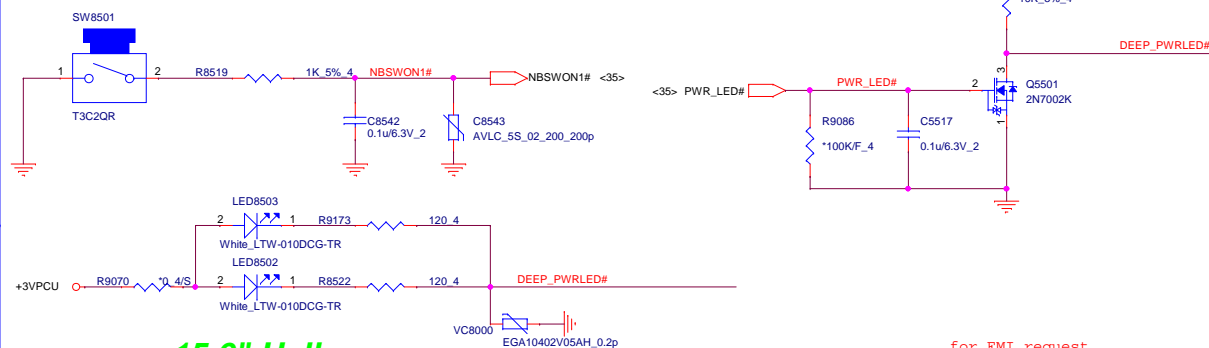
## Touch Pad



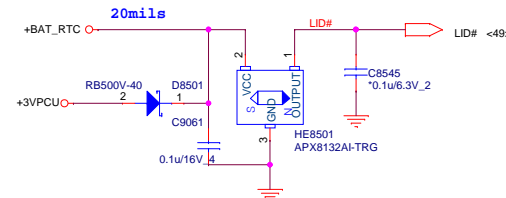
## FAN



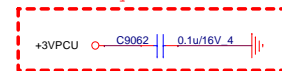
## PWR Button & LED & HALL IC



## 15.6" Hall sensor

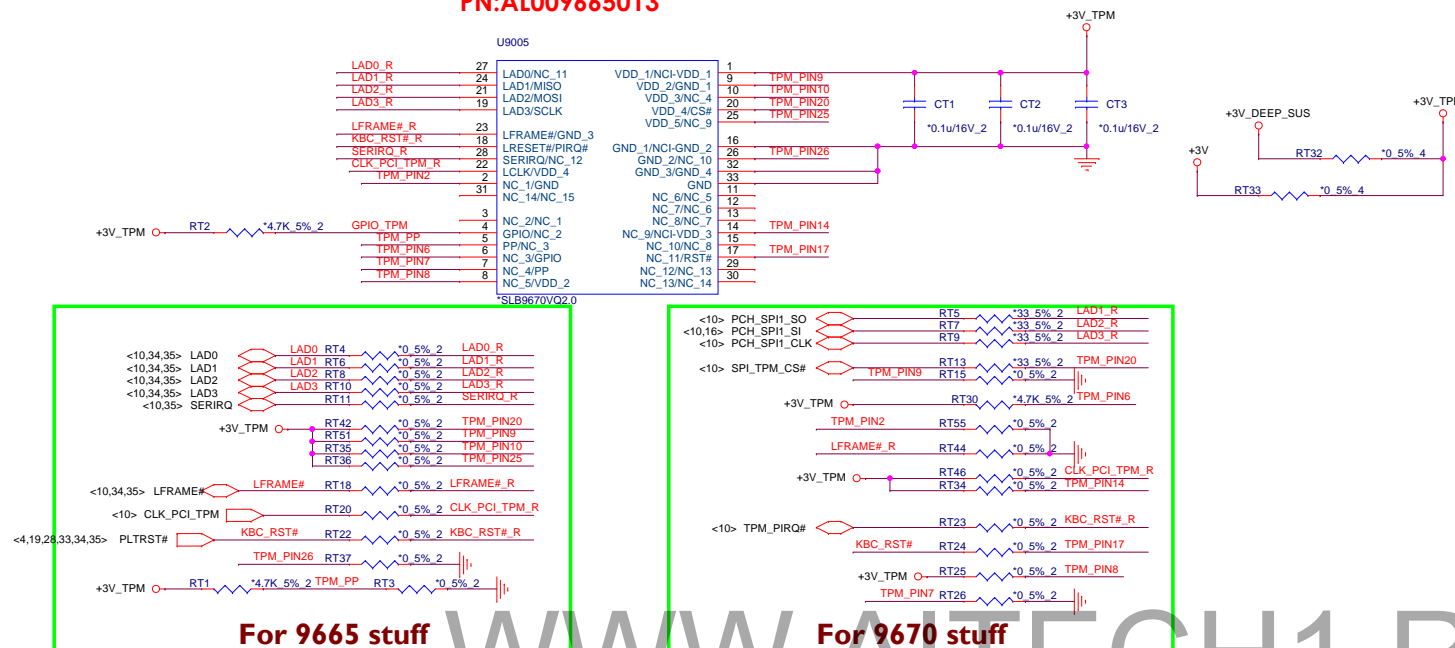


for EMI request

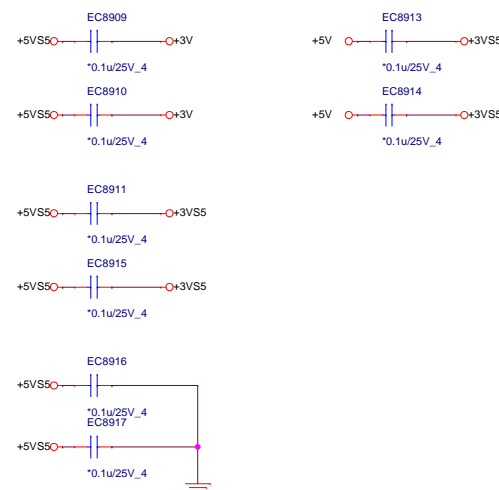
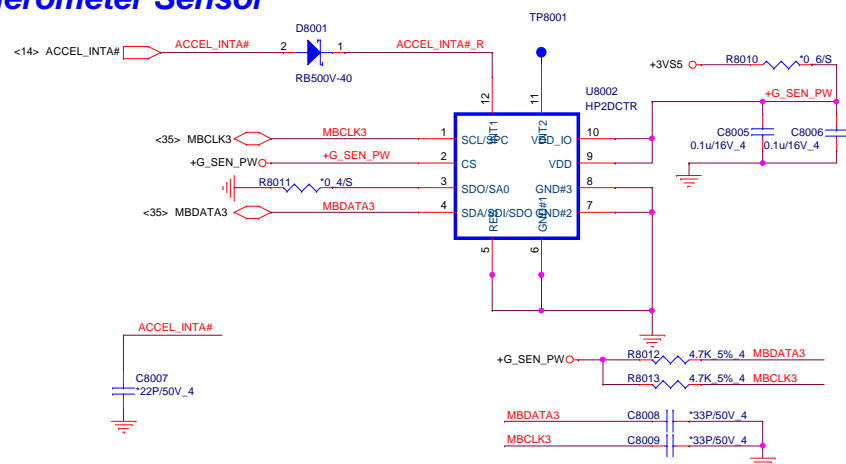


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**change to FW 5.6 I**  
**PN:AL009665013**

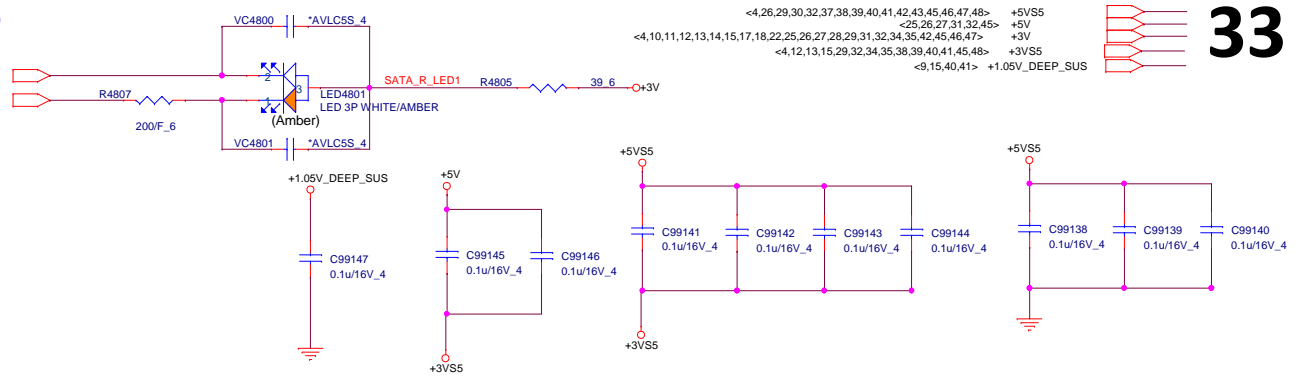
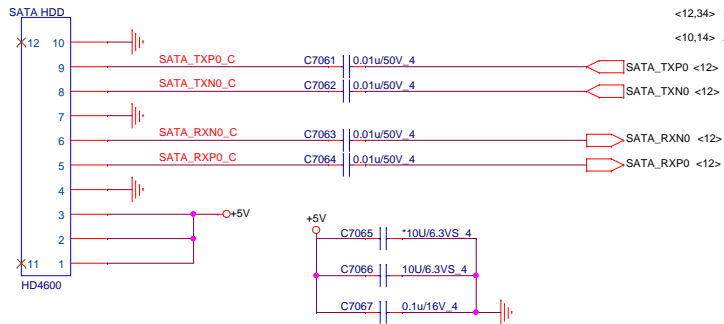


## EMI Solution

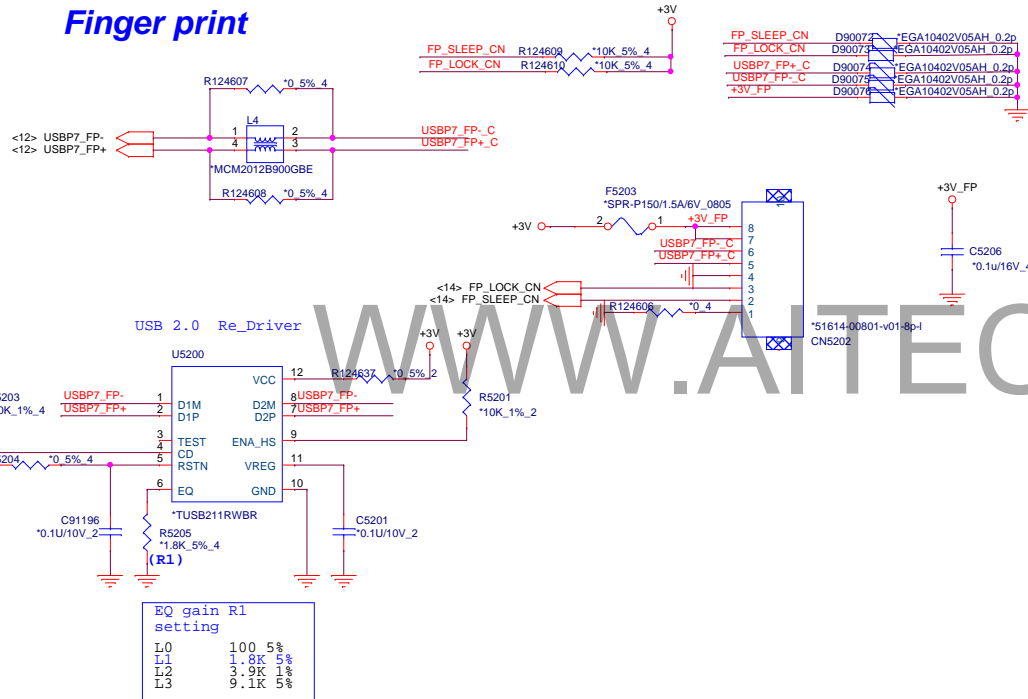


# SATA HDD & LED

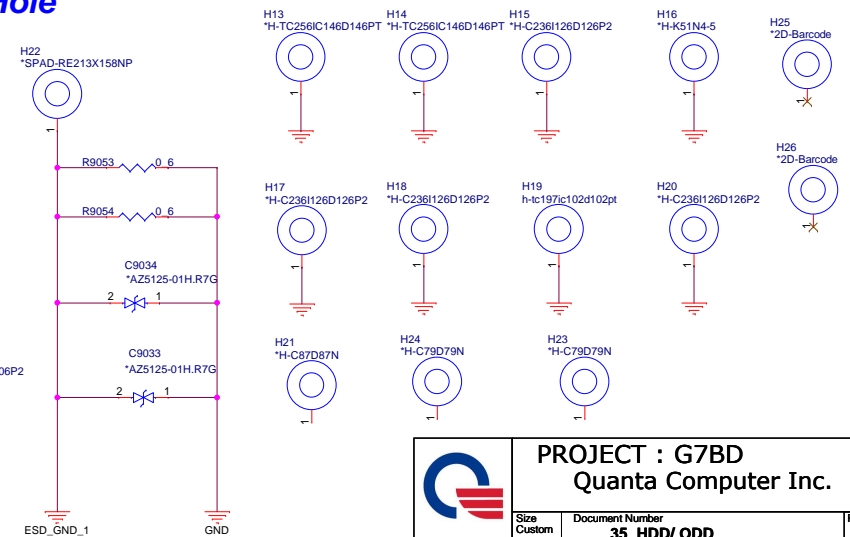
## SATA LED



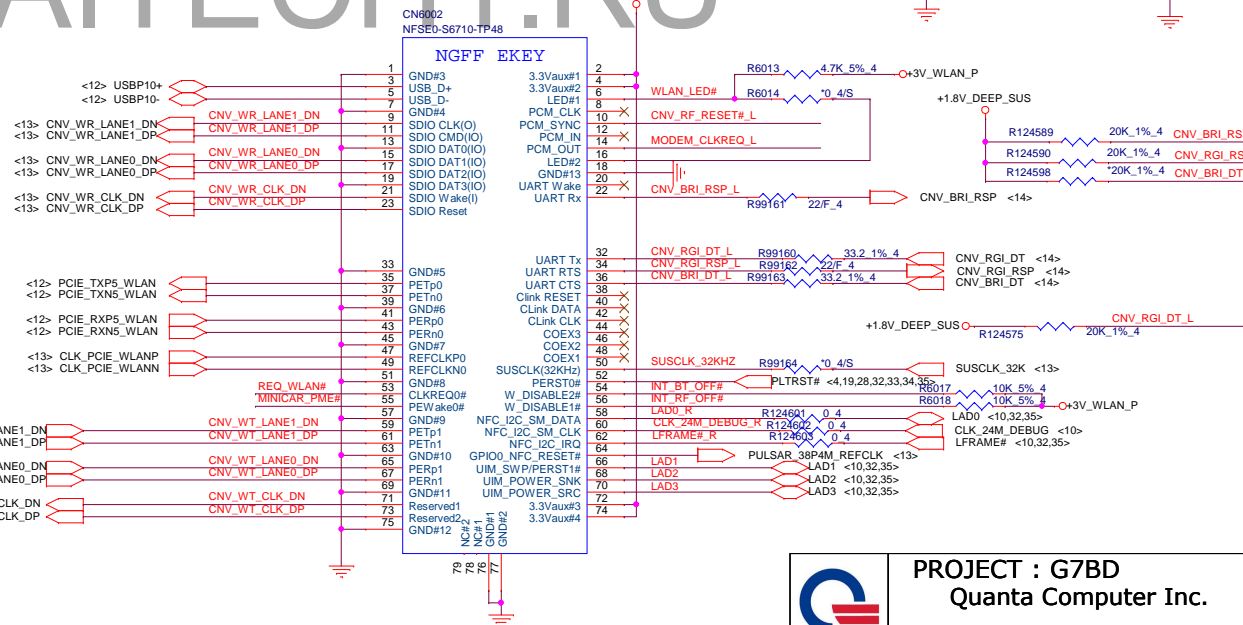
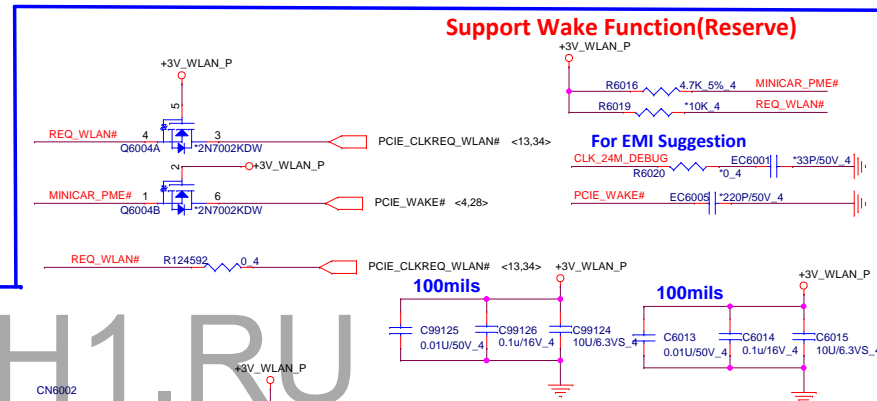
## Finger print

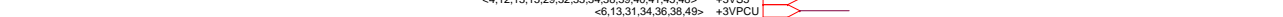


## Hole



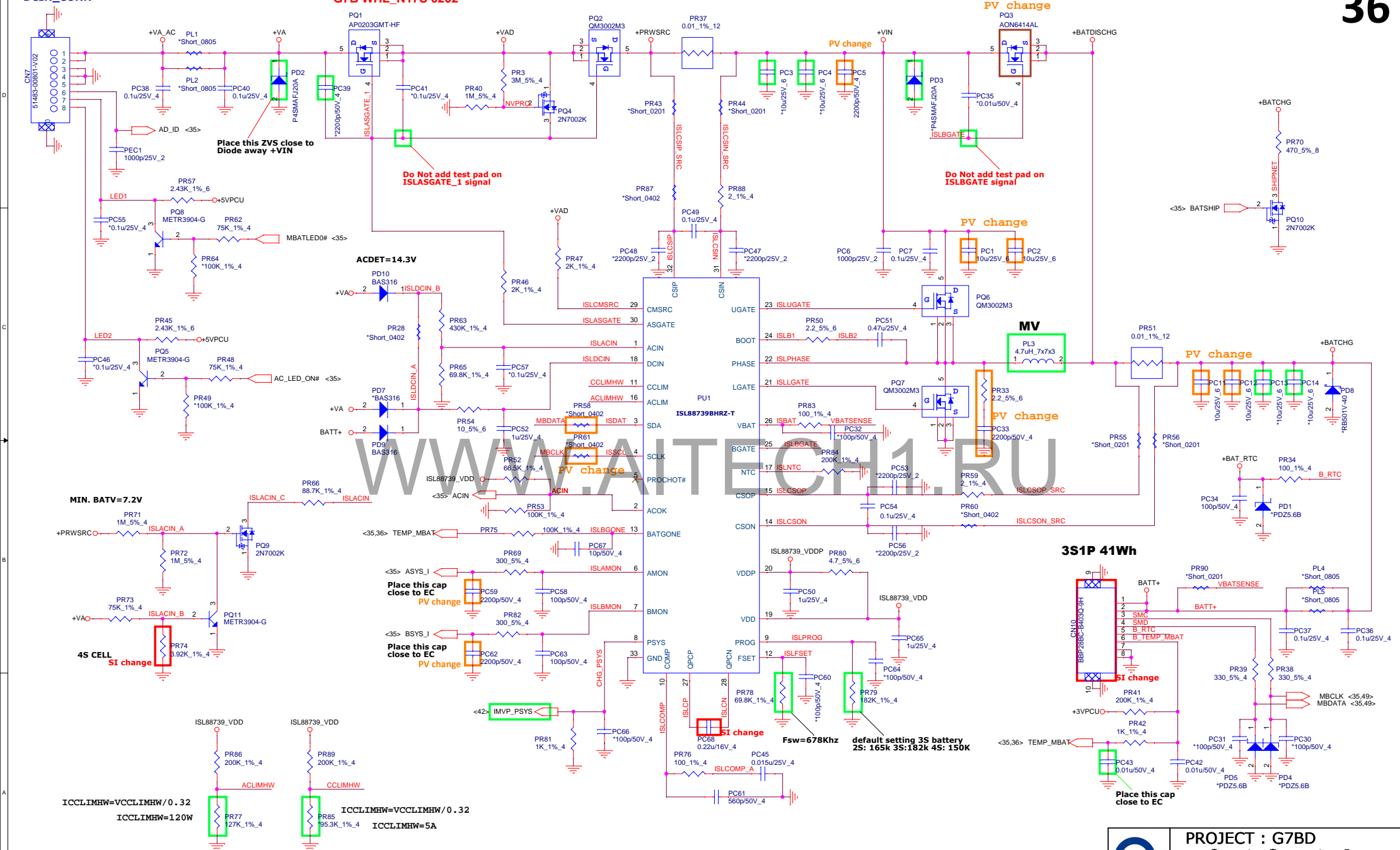
## 34



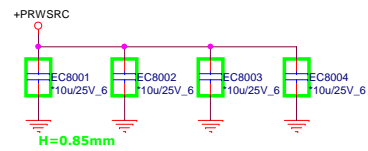


**DCIN CONN**

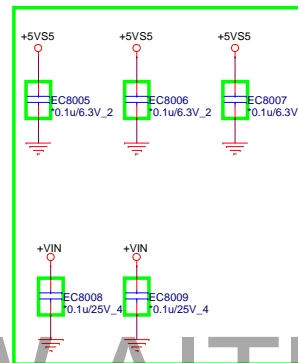
**G7B WHL N17S 0202**



Acoustic Solution



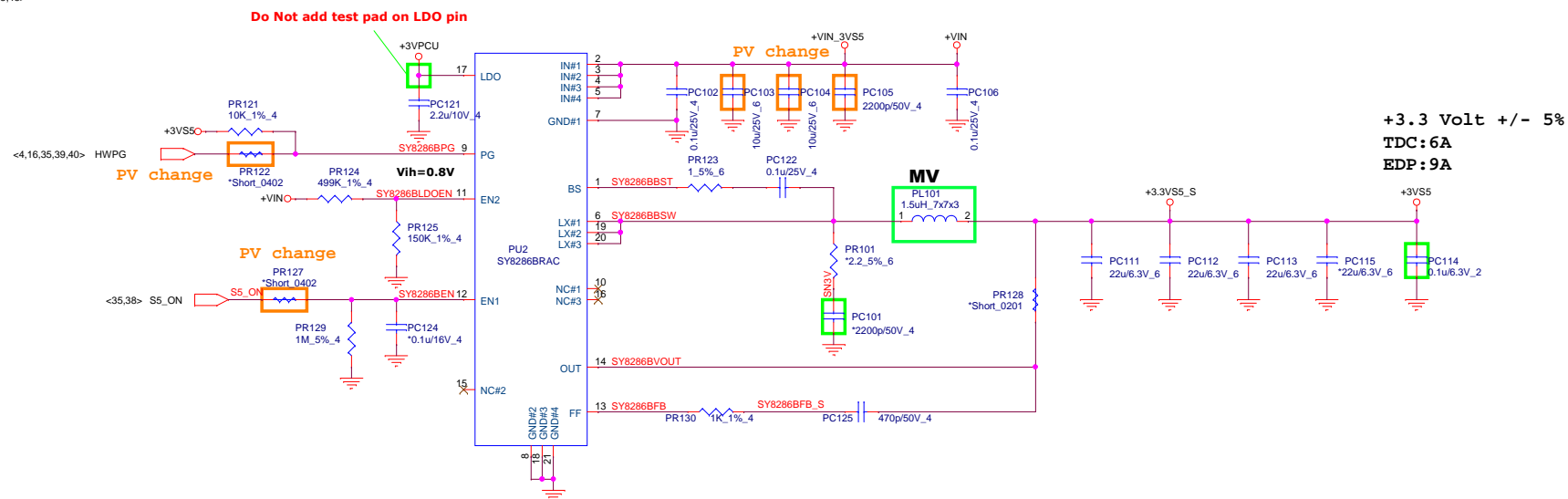
EMI suggestion to reserve



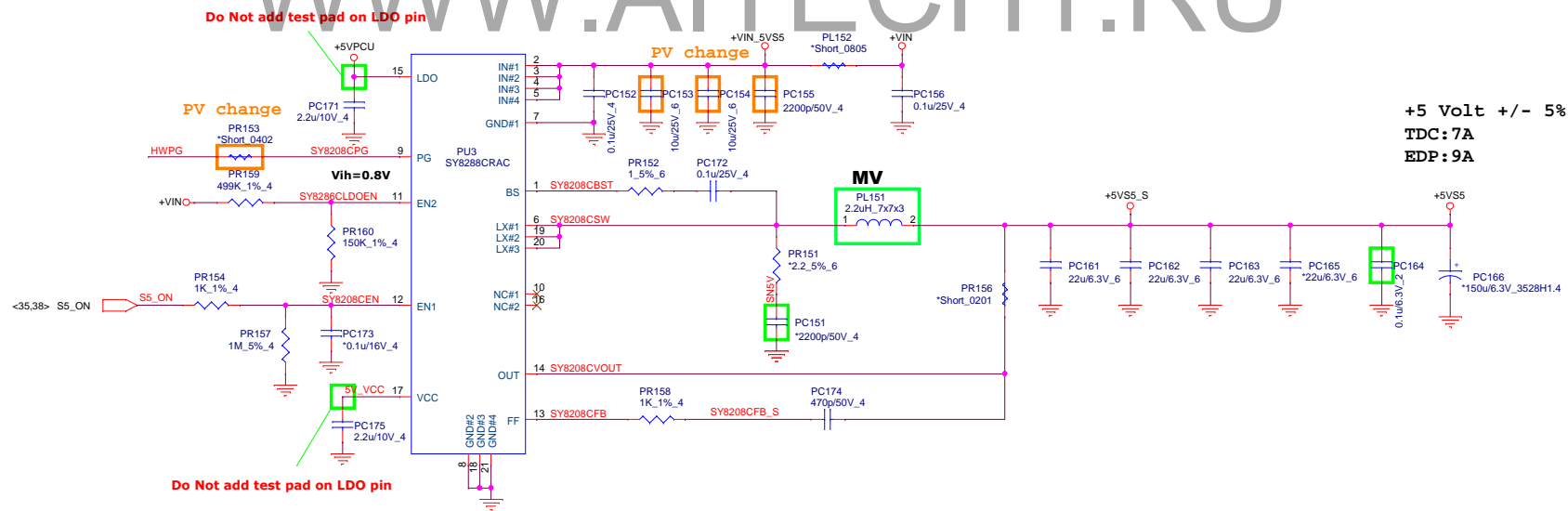
WWW.AITECH1.RU

## DC/DC +3VS5/+5VS5

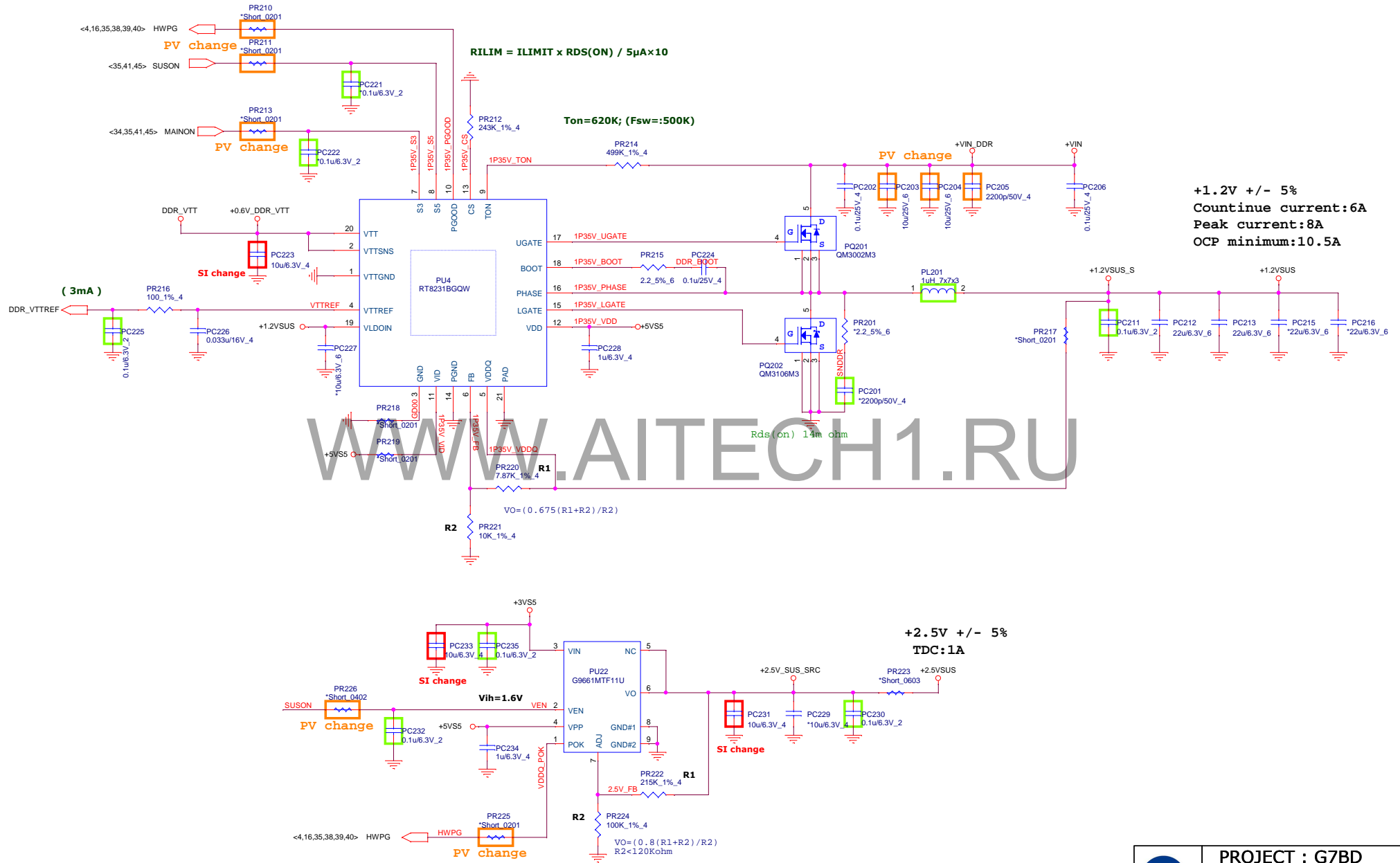
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 +3VS5 <4,12,13,15,29,32,33,34,35,39,40,41,45,48>  
 +5VS5 <4,26,29,30,32,33,37,39,40,41,42,43,45,46,47,48>  
 +3VPCU <6,13,31,34,35,36,49>  
 +5VPCU <28,34,36,45,48>



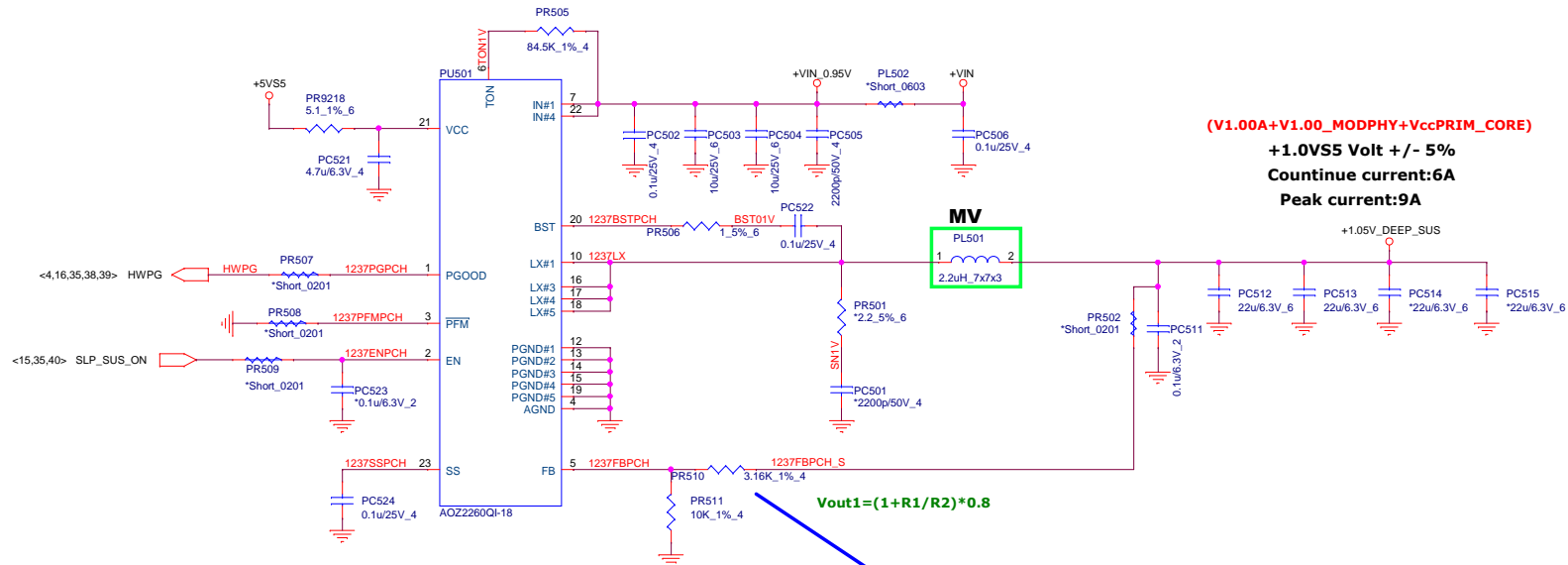
WWW.AITECH1.RU



+VIN <25,31,36,37,38,40,43,44,46,47>  
 +2.5VSUS <17,18>  
 +1.2VSUS <3,6,17,18,41>  
 DDR\_VTT <17,18>



Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

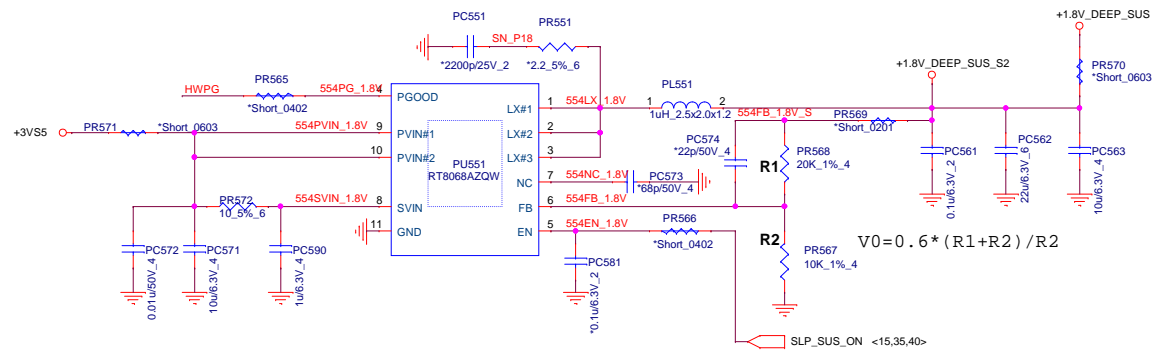


	1.91K	CS21912FB13	0.95V
SKL/KBL		CS22612FB15	1V
CNL/CFL/WHL	3.16K	CS23162FB04	1.05V

1.8VS5 +/- 3%

TDC: 3A

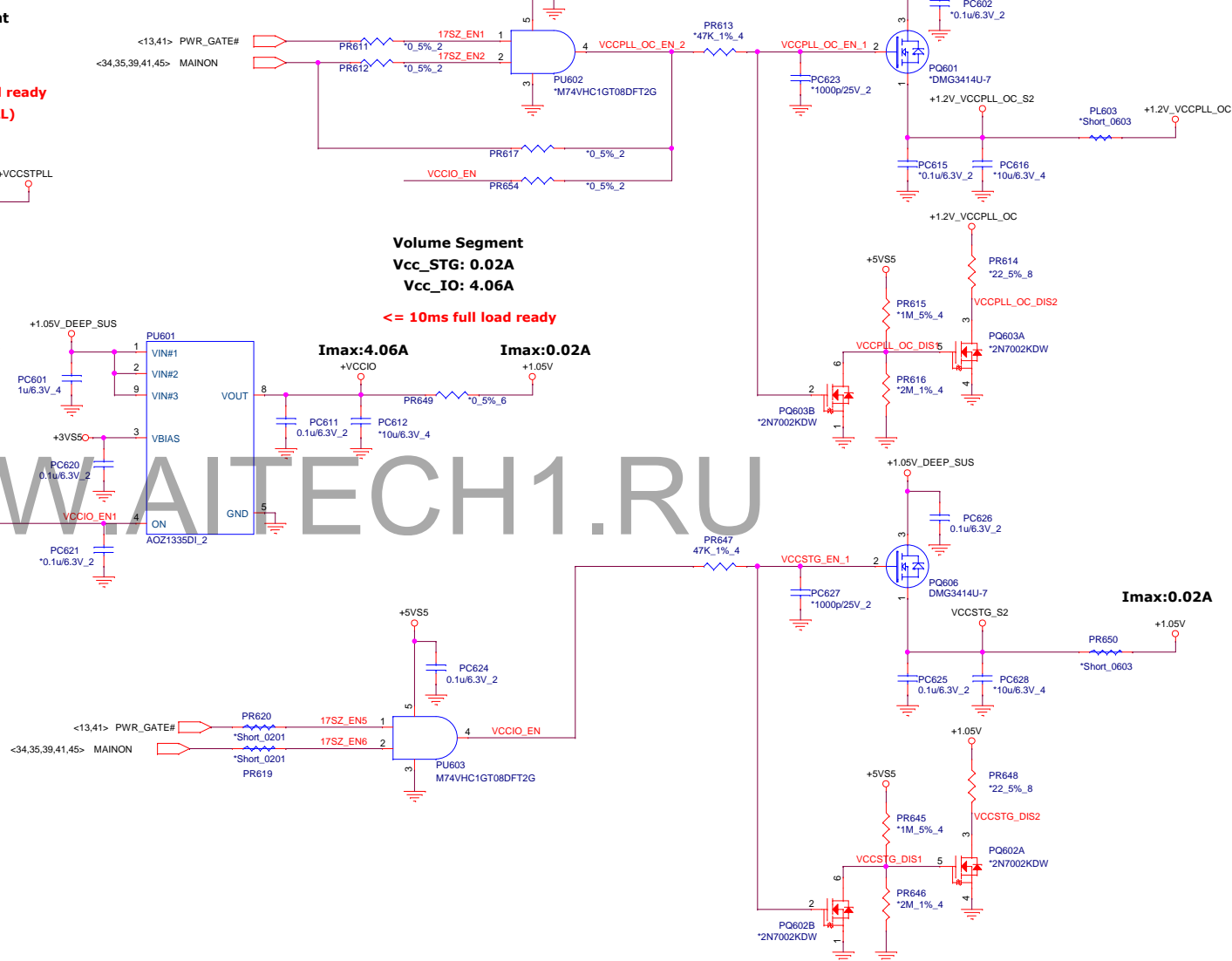
EDP : 4A

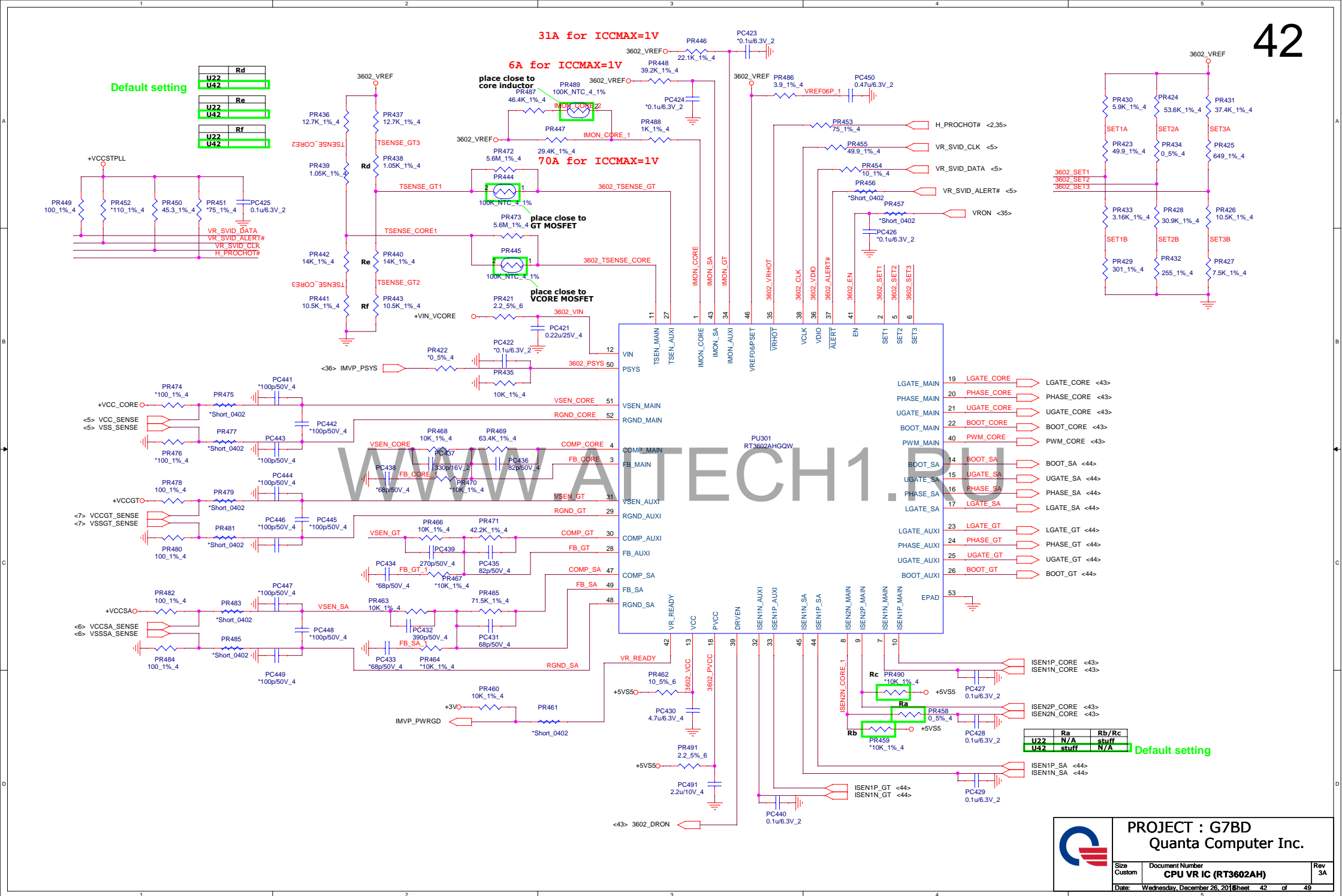


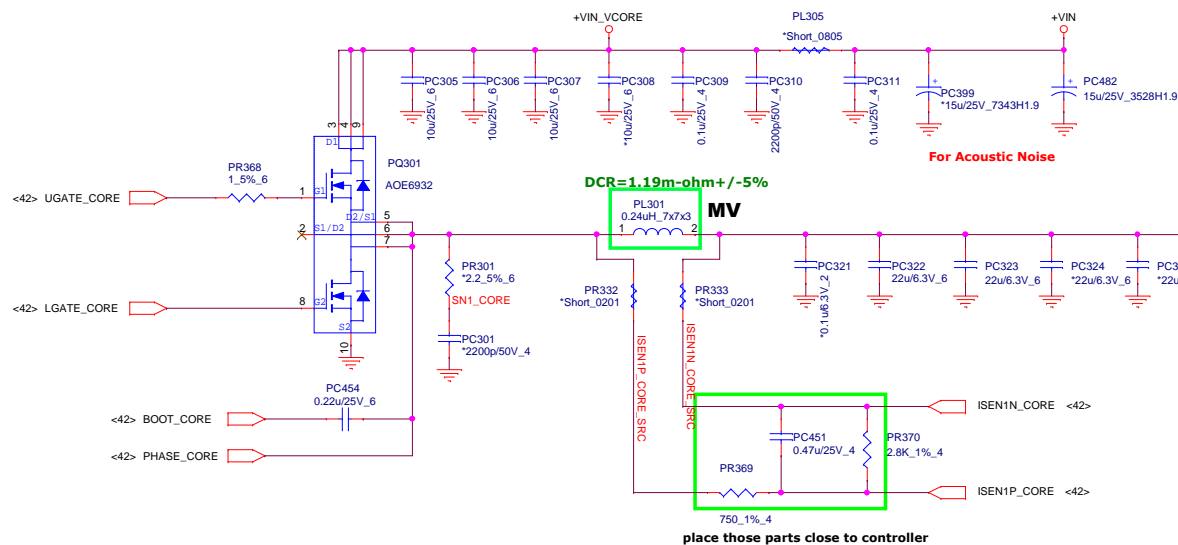
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Quanta Computer Inc.

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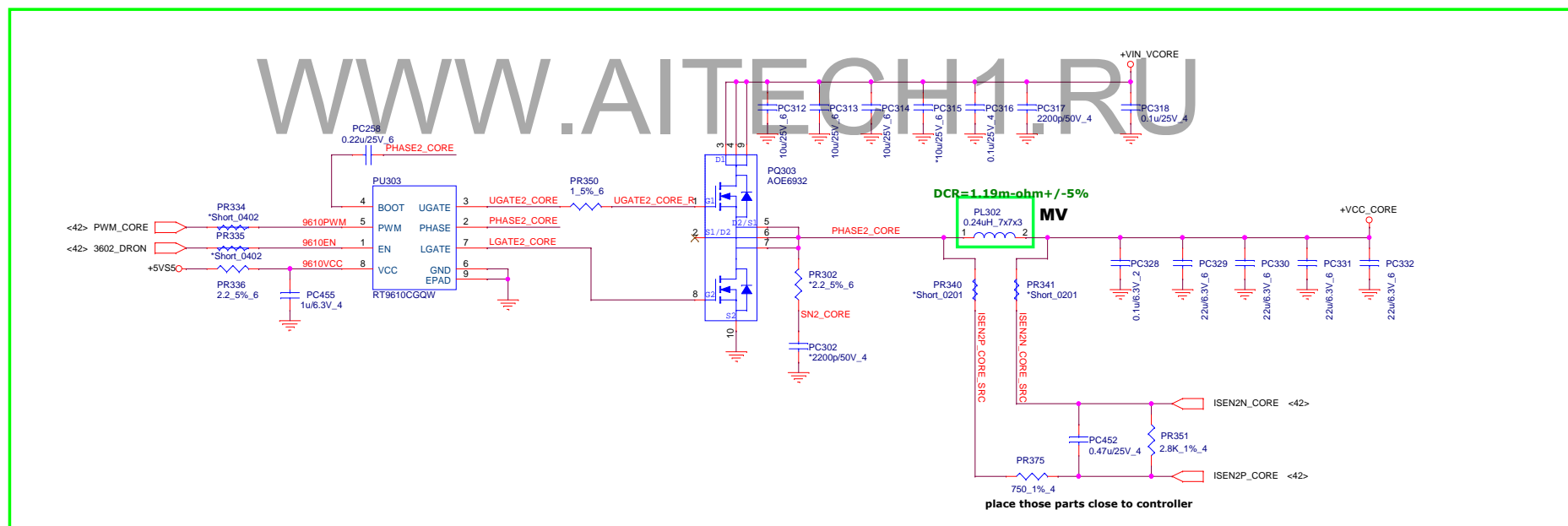
**TDC:0.26A**



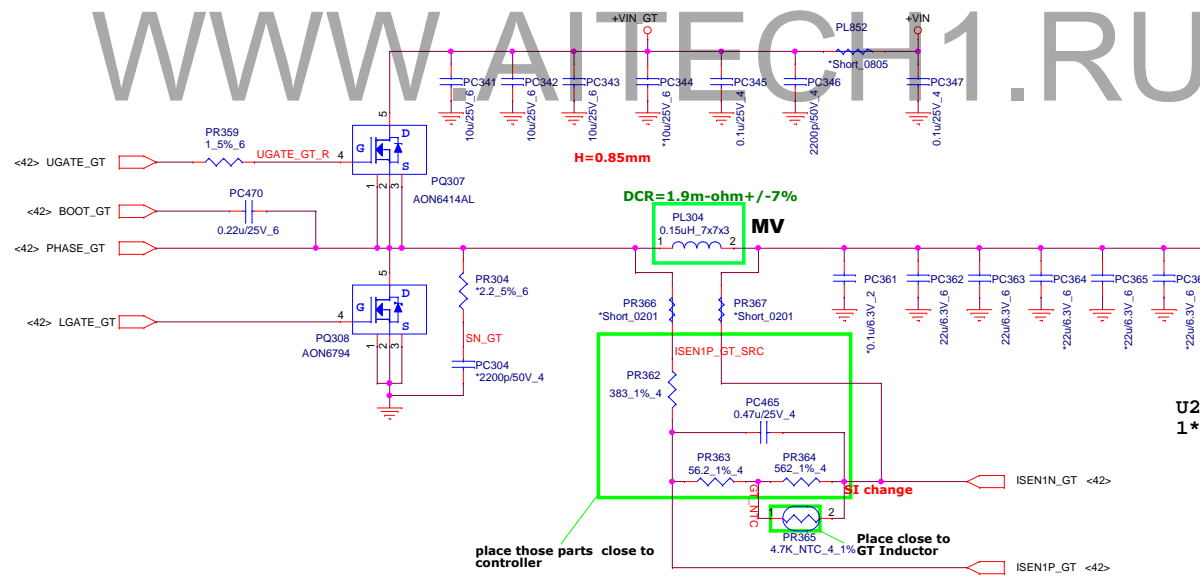
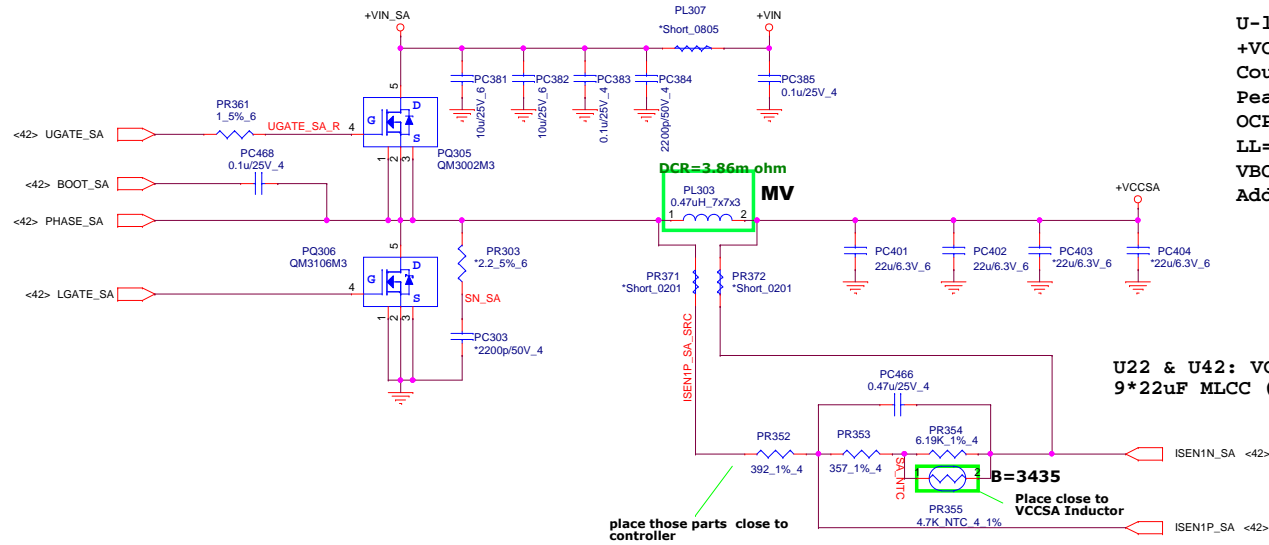


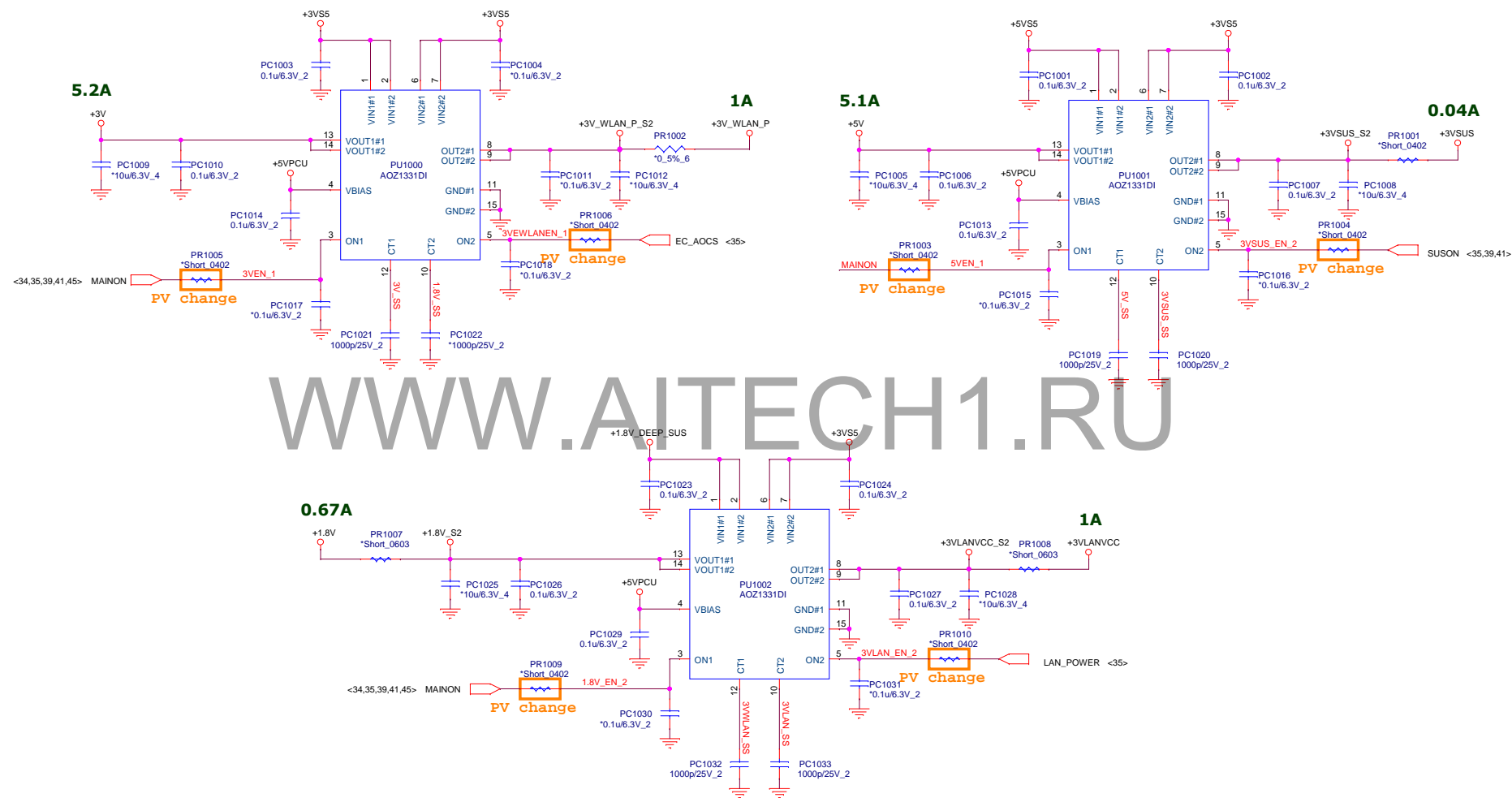


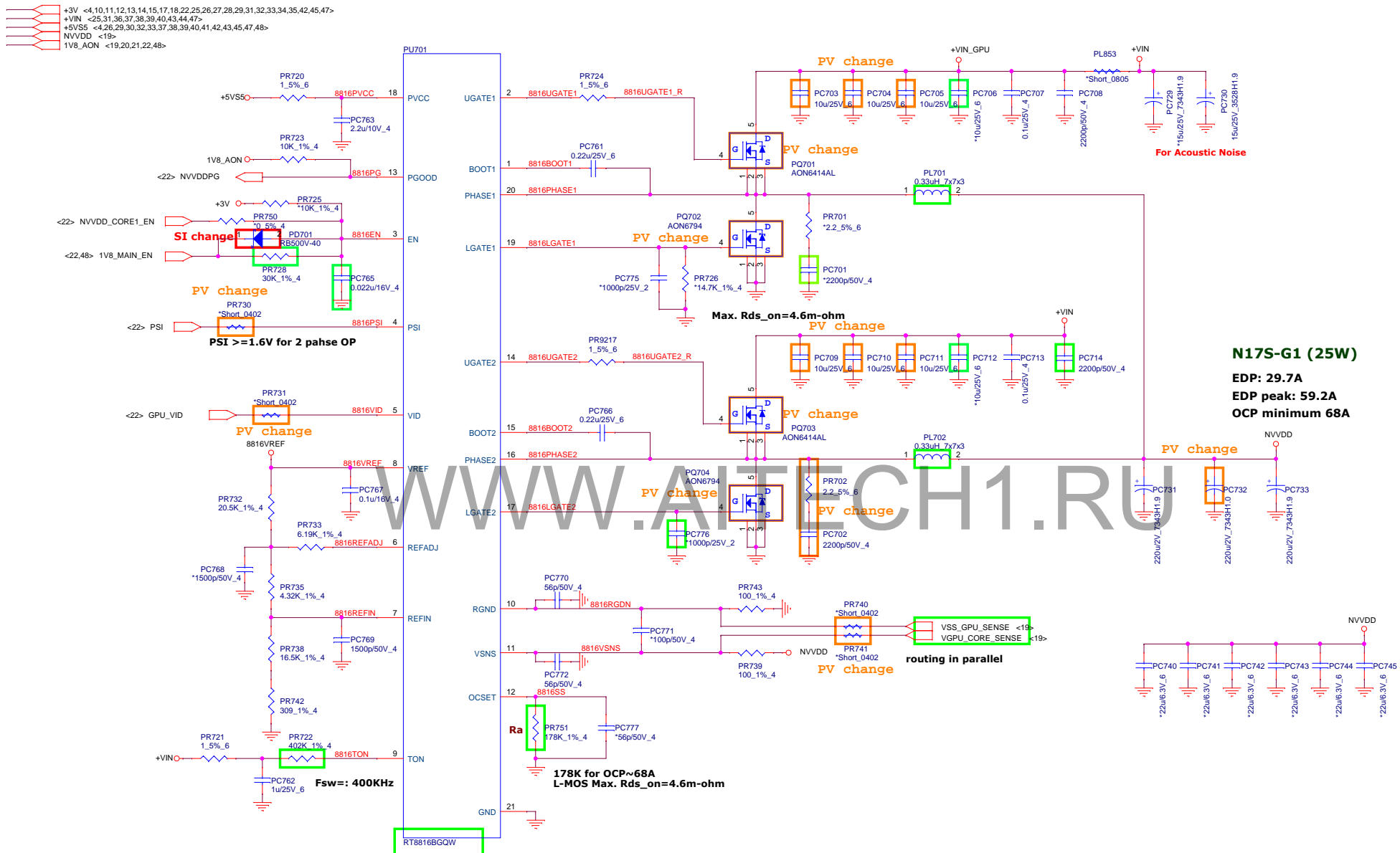
WHL U42: +VCC\_CORE  
2\*330uF/9m+33\*22uF MLCC (total with EE)



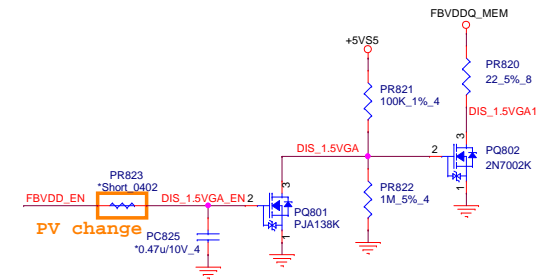
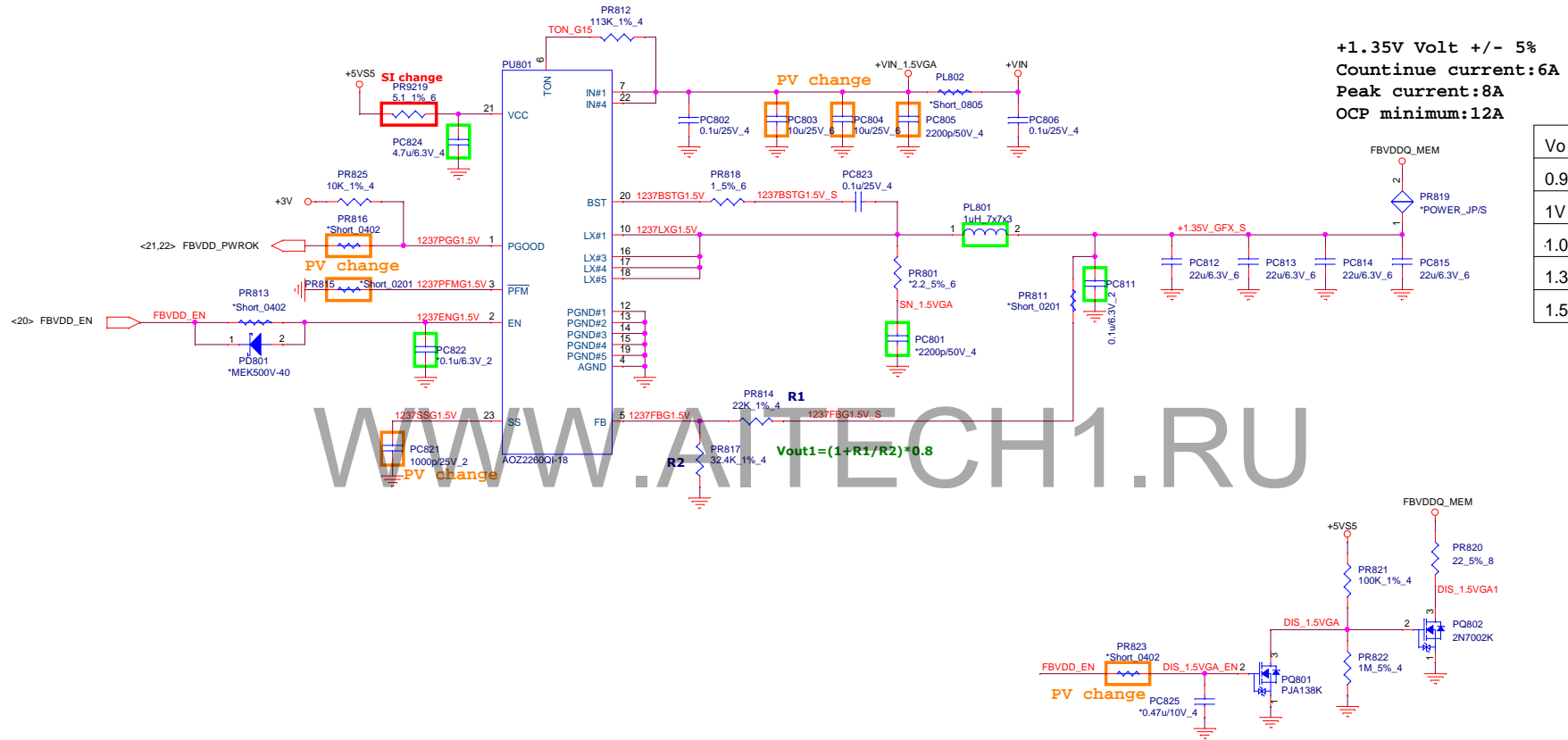
+VIN <25,31,36,37,38,39,40,43,46,47>  
 +5VSS <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,47,48>  
 +VCCSA <6,42>  
 +VCCGT <7,42>

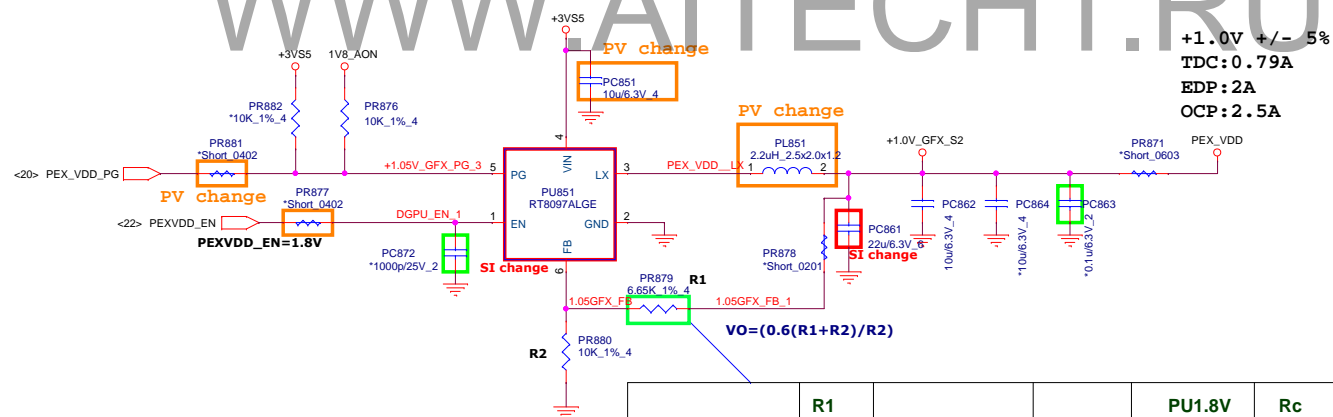
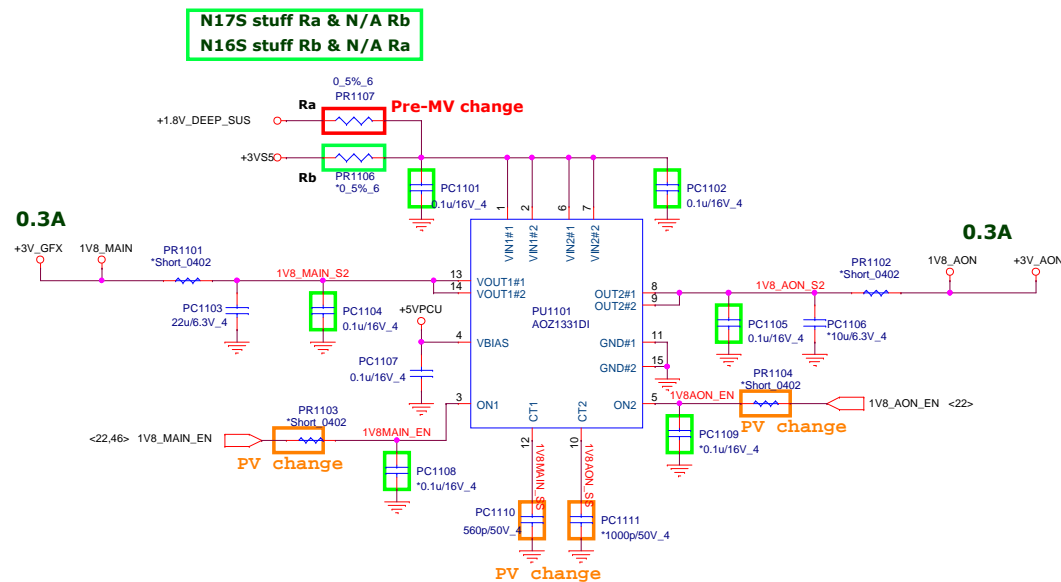
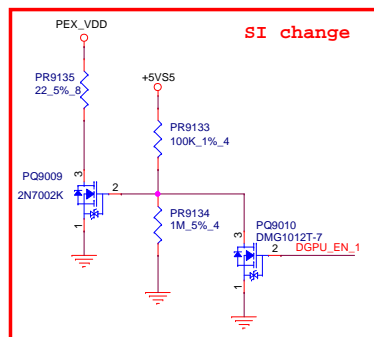




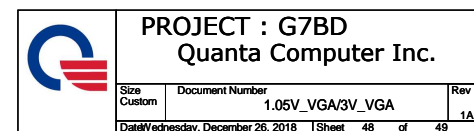


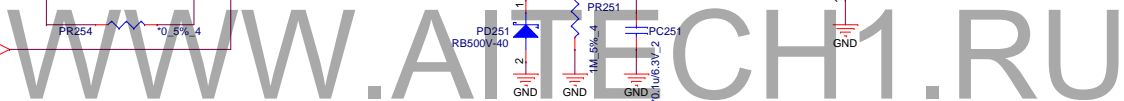
+VIN <25,31,36,37,38,39,40,43,44,46>  
 +5VS5 <4,26,29,30,32,33,37,38,39,40,41,42,43,45,46,48>  
 FBVDDQ\_MEM <20,21,23>





	R1			PU1.8V	Rc	Rd
N17P N17S	6.65K	CS26652FB06	1V	Unstuff	Unstuff	Stuff
N16S GTR	7.5K	CS27502FB11	1.05V	Unstuff	Stuff	Unstu





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